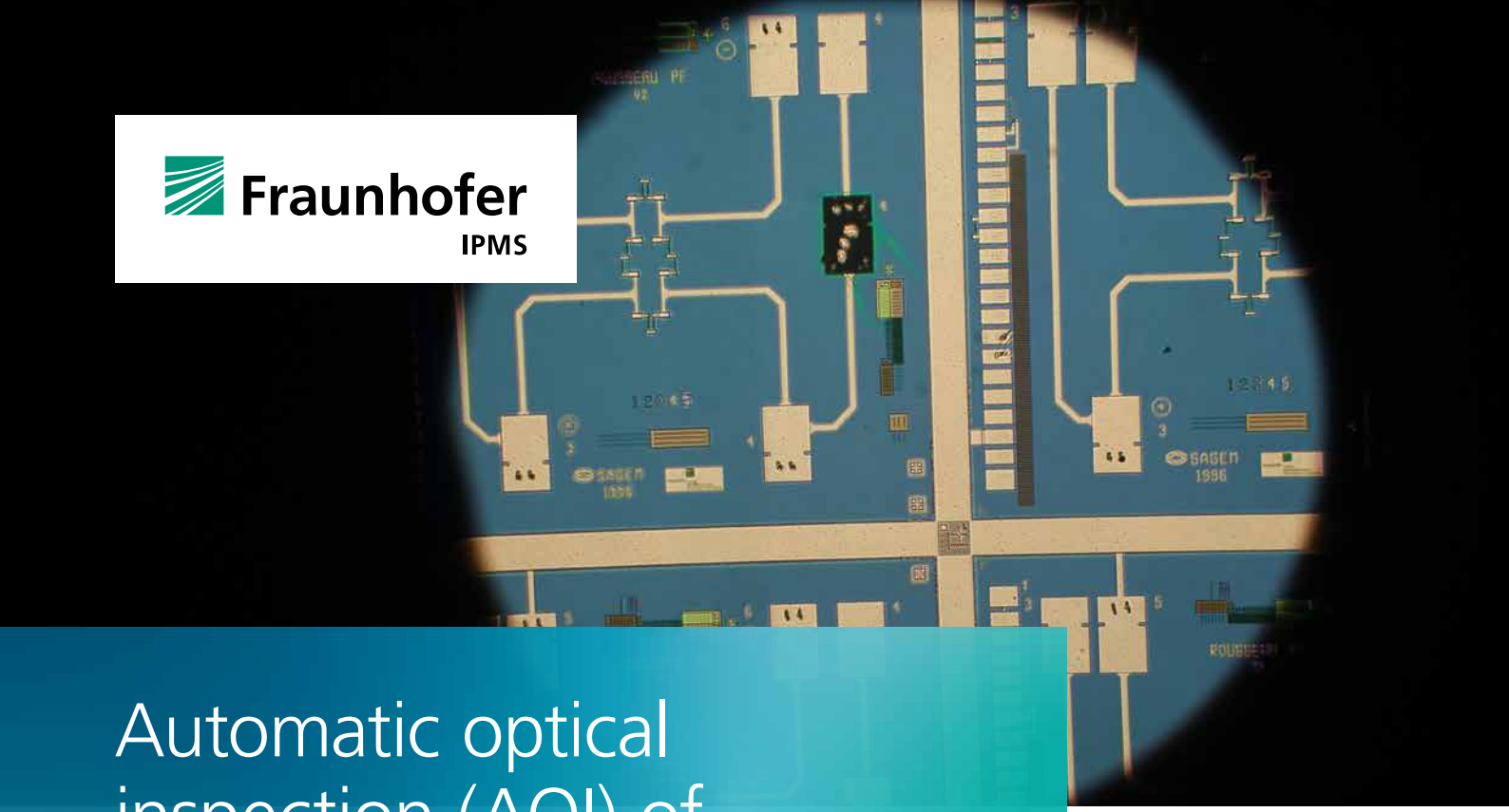
Fraunhofer IPMS



Automatic optical inspection (AOI) of microsystem chips

Inspection of a chip for possible defects.

Motivation

Fraunhofer IPMS develops and manufactures microsystem chips based on silicon wafers and technologies similar to those used in semiconductor production. The products often have optically or sensorically active surfaces or tiny mechanical structures where high quality is important, but which cannot be electrically tested. Therefore, an optical inspection of these regions is required for quality assurance, which complements the result of the electrical test.

Small quantities of such chips can be visually inspected and selected under a microscope. However, this method is no longer effective for large quantities. In addition, the result depends heavily on the person performing the test, their current concentration and condition. Fraunhofer IPMS has therefore developed and set up test equipment that automatically inspects microsystem wafers optically.

As wafer testers are equipped with a computer-controlled precision cross table and an alignment microscope, it made sense to adapt digital image acquisition technology and implement the optical tests using product-specific image processing programs.

Hardware

The optical tester consists of a PA-200 wafer prober from SUSS MicroTec AG, a Mitutoyo FS70Z microscope with M Plan Apo 5x objective for a large working distance, an A102fc digital IEEE 1393 camera from BASLER AG and a standard PC with a Matrox frame grabber. The cross table has a wafer holder for different wafer types. Only the loading and unloading of the wafer still has to be carried out manually; however, it can potentially also be automated.

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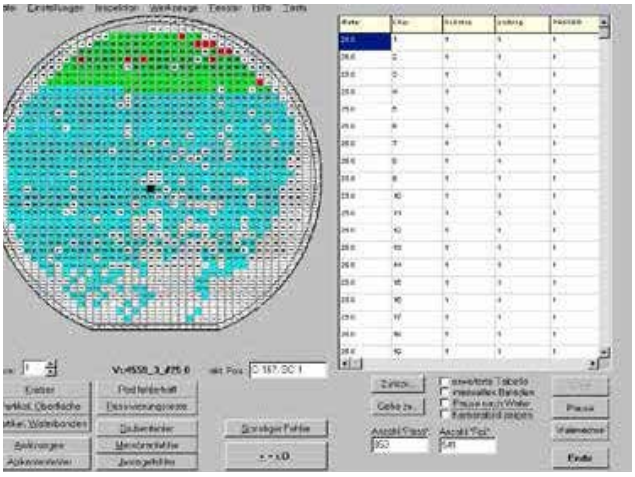
Photo of the automatic optical inspection station at Fraunhofer IPMS



VITool snapshot of a running test: Good chips are green, faulty chips are marked red, blue chips have not yet been tested.

Software

The optical test software called VITool (Visual Inspection Tool) controls the cross table movement according to the chip positions and the acquisition of the required images. For image processing, the product-specific algorithm provided as a Dynamic Link Library (DLL) is called up, which draws on the MATROX MIL Imaging Library. The interface between the two layers is defined in such a way that all test options and parameters can be modified interactively or via configuration files without changing the program code itself.

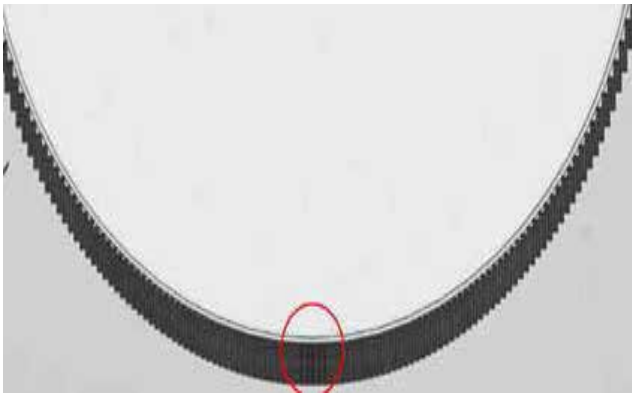
After the complete evaluation, the binary result of the optical test – pass (good chip) or fail (defective chip) – is entered in the wafer's chip table (wafer map). Each chip must pass both the electrical and optical tests in order to be further processed as a good chip. The VITool software has a graphical user interface (see top right image) in which the test progress and yield trend are visible during processing.

With some microsystem chips, very fine structures need to be examined optically, which cannot be resolved in one image over the entire chip surface. In this case, the chip must be partitioned, e.g. one half or one quarter of each partial image is captured and then positioned for the next partial image using the cross table. Before the image is analyzed, the partial images are then combined to form an overall image. The image on the bottom right shows such a partial structure as an example.

Applications

The optical test equipment described here is used, for example, for quality control of the following products that Fraunhofer IPMS manufactures for its key customers:

- Micro-(opto-) electro-mechanical systems (MEMS / MOEMS) devices
- Multi-field photodetectors for optical measurement systems
- Organic light-emitting diodes (OLEDs), including for testing the homogeneity of light emission



Fine comb structure of a MEMS that requires sub-image processing.