Fraunhofer CNT

FRAUNHOFER CENTER NANOELECTRONIC TECHNOLOGIES

JAHRESBERICHT

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CONTENTS

Preface 4

Fraunhofer Center Nanoelectronic Technologies Overview

- Profile 8
- Figures 12
- Cooperation 16

Competence Areas and Research Results 19

- Analytics 20
- Functional Electronic Materials - Front End of Line 26
- Functional Electronic Materials - Back End of Line 32
- Maskless Lithography 40
- Devices & Integration 46

Events 54

Publications 59

Contact 64

Editorial Notes 65

PREFACE

Director: Prof. Dr. Peter Kücher

Für das Fraunhofer Center Nanoelektronische Technologien (CNT) war 2011 ein erfolgreiches Jahr, in dem einige Rahmenbedingungen für die zukünftige Entwicklung geschaffen wurden.

Die lange Zeit der Ungewissheit seit 2009 bezüglich der angemieteten Reinraum-, Labor- und Büroflächen nach der Insolvenz des Industriepartners Qimonda, wurde mit dem Erwerb des ehemaligen Qimonda-Geländes durch Infineon im Juni 2011 beendet. Infineon hat das Interesse bekundet, die Flächen auch weiterhin an Fraunhofer zu vermieten und standortbezogene Dienstleistungen anzubieten. Die Verhandlungen dazu sollen in 2012 abgeschlossen werden. In einem umfassenden Strategieprozess haben wir langfristig die Kernkompetenzen und Geschäftsfelder neu definiert sowie die Ziele festgelegt. Der Jahresbericht gibt Ihnen dazu einen guten Überblick. Besonders erfreulich ist die Zunahme von Aufträgen, neben großen IC-Herstellern, gerade von mittelständischen Unternehmen und Start-up Firmen, die unabhängig von Förderprojekten direkt an die Einrichtung erteilt wurden und in diesem Jahr, den Umfang von nahezu einer Million Euro erreichten. Dies ist einmal mehr der Beweis für die Wertschätzung der vorhandenen Kompetenzen und die Erkenntnis, dass die Ergebnisse aus der Nanoelektronik zunehmend Anwendungen auch in Systemen der Mikroelektronik finden gemäß dem Motto „Nano for Micro“. Mein besonderer Dank geht an die Auftraggeber, die das Fraunhofer CNT auch in den turbulenten vergangenen Jahren als zuverlässigen Forschungsdienstleister geschätzt haben, woraus sich auch einige längerfristige Partnerschaften entwickelten.

Als Beispiel sei hier ASM International genannt. Nach mehreren Jahren vertrauensvoller Zusammenarbeit konnte mit diesem international führenden Anlagenhersteller eine längerfristige, bilaterale Kooperation im Bereich Atomlagenabscheidung (ALD) und Epitaxie abgeschlossen werden. Unsere Kompetenz im Bereich Prozesse, Materialien und Anlagen soll zukünftig durch weitere Kooperationen ausgebaut werden. Als ein beständiger Partner für Entwicklungsprojekte erwies sich unser Industriepartner GLOBALFOUNDRIES. Durch dessen deutliche Verbreiterung des Technologie- und Produktportfolios als Foundry ergaben sich zusätzliche Anknüpfungspunkte für Industrieaufträge, die erfolgreich zum Abschluss gebracht wurden. Zudem sind neue Forschungsinhalte definiert worden. Mehrere Projekte und Vereinbarungen konnten zudem mit anderen IC-Herstellern, IP-Firmen und Anlagenherstellern sowohl im Bereich Abscheidung, Hoch-Temperatur Behandlung als auch bei Testsystemen z.B. mit der Firma Tokyo Elektron (TEL) getroffen werden. Seit Mitte 2011 konnte das Fraunhofer CNT auf eine Grundfinanzierung zurückgreifen. Damit wurden unter anderem die vorhandenen Kompetenzen für MIM (Metall-Isolator-Metall) Kondensatorstrukturen, z.B. für Pufferspeicher in Analog/Digital Mixed Signal Bausteinen oder in mikroelektronischen Systemen, weiterentwickelt.

Durch die vom Land Sachsen geförderten Projekte in den Geschäftsfeldern „Enabling 300mm Production“ und „Nanopatterning“ sowie „Innovative Materialien und Prozesse für die Nano-und Mikroelektronik“ konnte die herausragende Qualität und das Potential der etablierten Technologien gerade in der breiten Anwendung für die Mikrosystemtechnik und Nanoelektronik bei Strukturen unter 30 nm demonstriert werden. Durch diese Projekte hat die Einrichtung wesentlich dazu beitragen, Innovationen in den „Key Enabling Technologies“ voranzutreiben, wie in einer EU Kommunikation im September 2009 „Preparing for our future: Developing a common strategy for key enabling technologies in the EU"{SEC(2009) 1257} beschrieben.
Damit liefert das Fraunhofer CNT auch weiterhin einen wesentlichen Beitrag für die herausragende Stellung Dresdens als Mikroelektronik-Standort in Europa, als Bindeglied zwischen „More Moore“ und „More than Moore“ Technologien und Anwendungen. Besonders

2011 was a successful year for Fraunhofer Center Nanoelectronic Technologies (CNT) in which the framework for future development has been created.

The long period of uncertainty since 2009 regarding the rented cleanroom, laboratory and office space followed by the insolvency of industry partner Qimonda, has been completed with the acquisition of Qimonda's properties by Infineon in June 2011. Infineon has expressed an interest in further collaborations with Fraunhofer by providing facilities and location-based services. The negotiations should be completed in 2012. Long-term core competencies, business areas and goals have been established in a comprehensive strategy process. This annual report gives you a good overview.

Particularly pleasing is the increase of orders, from major IC manufacturers and especially from medium-sized companies and start-up companies which were granted, regardless of funding projects, directly to the institution. This year, the amount has reached nearly one million Euros. This is another proof of the appreciation of the CNT competencies and the evidence that results from nanoelectronic research increasingly find applications in microelectronics systems in accordance with the slogan "Nano for Micro."

My special thanks goes to the authorities who have valued the Fraunhofer CNT as reliable research service provider in the turbulent last years from which, also some longer-term partnerships have developed. As an example, ASM International is mentioned. After several years of faithful cooperation with this leading international equipment manufacturer, a longer-term bilateral cooperation in the field of atomic layer deposition (ALD) and epitaxy is completed. Our expertise in processes, materials and equipment is planned to be expanded through further cooperation.

A steady partner for development projects is our industry partners GLOBALFOUNDRIES. Its significant broadening of the technology and product portfolio as a foundry resulted in additional industry orders that have been completed successfully. In addition, new research content has been defined. Several projects and agreements were also made with other IC manufacturers, IP companies and equipment manufacturers in the field of deposition, high-temperature treatment as well as in test systems with the company Tokyo Electron (TEL).

Since mid-2011, Fraunhofer CNT can rely on core funding. Among other things, this was used to develop the existing competencies for MIM (metal-insulator-metal) capacitor structures, e.g. for buffer memory in analog / digital mixed signal ICs or in microelectronic systems evolved.

By the state of Saxony-funded projects in the fields of "enabling 300mm Production" and "Nanopatterning" and "Innovative materials and processes for nano-and microelectronics" the outstanding quality and the potential of established technologies currently in wide use for microsystems technology and nanoelectronics were demonstrated in structures below 30 nm.

Through these projects, the Fraunhofer CNT was able to significantly push innovations in the "Key Enabling Technologies" forward, stated in an EU Communication in September 2009 "Preparing for our future: Developing a common strategy for key enabling technologies in the EU" {SEC (2009) 1257}.For this reason the Fraunhofer CNT continues to contribute to the prominent position of Dresden as a microelectronic location in Europe, as a link between "More Moore" and "More than Moore" technologies and applications.

Particularly encouraging, the conclusion of two other promotions at Fraunhofer CNT with the subjects:

PREFACE

erfreulich war auch der Abschluss von zwei weiteren Promotionen im Fraunhofer CNT mit den Themen: Kinetik der elektrochemischen Kupferabscheidung in Sub-100 nm-Strukturen und der Analyse von High-k Materialien mittels Atom Probe. Alle Doktoranden bestätigten die Effektivität mit der die Arbeiten, gerade durch die enge Zusammenarbeit mit der Industrie und den betreuenden Professoren, durchgeführt werden konnten. Viele Mitarbeiter und Mitarbeiterinnen haben sich im Laufe des Jahres z.B. bei der „Langen Nacht der Wissenschaften" oder beim Praktikum von Schülern, z.B. des Martin-Andersen-Nexö Gymnasiums engagiert.
Am 2. November fand der zweite „Fraunhofer CNT Research Day" statt. Dafür konnten wir mehrere Experten mit Beiträgen von führenden Unternehmen wie z.B. Infineon, STMicroelectronics, ASM und CEA-Leti, Air Liquide begrüßen, die neben Wissenschaftlern aus unserem Institut neueste Erkenntnisse und Strategien auf verschiedenen Fachgebieten vorstellten. Die große Beteiligung mit nahezu 100 Teilnehmern und das positive Feedback der Gäste sind Motivation, diese Veranstaltung auch im nächsten Jahr fortzuführen. Als Auszeichnung für die wissenschaftliche Kompetenz am CNT dürfen wir die Entscheidung werten, den 17th Workshop on Dielectrics in Microelectronics (WoDiM) vom 25.- 27.6.2012 ausrichten zu dürfen.

Die Einrichtung wurde mit ihren Kompetenzbereichen und der Ausrichtung auf neue Anwendungsfelder optimiert aufgestellt. Für das Jahr 2012 und darüber hinaus ermöglicht dies ein weiteres Wachstum und lässt uns positiv in die Zukunft schauen. Dies verdankt das Fraunhofer CNT engagierten und kompetenten Mitarbeitern und Mitarbeiterinnen sowie unseren Partnern aus der Industrie, anderen Forschungseinrichtungen und Instituten, denen ich an dieser Stelle besonders für das entgegengebrachte Vertrauen danken möchte.

kinetics of electrochemical deposition of copper in sub-100 nm structures and the analysis of high-k materials with Atom Probe. All students confirmed the effectiveness of their work through a close cooperation with the industry and the supervising professors. Many staff members were engaged in activities such as the "Night of Science" or the internship of students e.g. from the "Martin Andersen Nexo"-school.

On November 2nd the second "Fraunhofer CNT Research Day" took place with several experts from leading companies such as Infineon, STMicroelectronics, ASM and CEA-Leti, Air Liquide and researchers from our institute who presented the latest results and strategies in various fields. The large turnout with about 100 participants and the positive feedback from guests are motivation to continue this event again in 2012. As recognition of the scientific expertise at the CNT, we evaluate the decision, to host the 17th Workshop on Dielectrics in Microelectronics (WoDiM) June 25 - 27, 2012 in Dresden.

The facility has been optimized regarding its competence areas and new fields of applications. For the year 2012 and beyond, this allows further growth and a positive perspective for the future. I would like to use this opportunity to thank our highly motivated and competent employees as well as all our business partners and supporters for their confidence.

Prof. Dr. Peter Kücher

PROFILE

Forschung und Entwicklung im Fraunhofer CNT

Das Geschäftsfeld des Fraunhofer CNT umfasst die Entwicklung von Prozessschritten und Materialien sowie die physikalische und elektrische Charakterisierung für High-Performance-Logik, Derivate (z. B. embedded DRAM) und Speichertechnologien für flüchtige und nicht-flüchtige Bauelemente.
Zielsetzung der Einrichtung ist es, innovative Einzelprozesslösungen für nanoelektronische Systeme vor allem auf 300 mm Wafern mit Industriepartnern und anderen Forschungseinrichtungen so zu entwickeln, dass diese schnell in ein industrielles Fertigungsumfeld übertragen werden können.

Das Leistungsangebot des Fraunhofer CNT basiert auf fünf Kompetenzbereichen:

- Analytik
- Funktionale Elektronische Materialien - Front End of Line
- Funktionale Elektronische Materialien - Back End of Line
- Devices & Integration
- Maskenlose Lithographie

Die Kompetenzbereiche forschen vor allem in den folgenden Geschäftsfeldern:

- Leading Edge Technologie für die Nano-Mikroelekt ronik
- Enabling 300 mm Production
- Nanostructuring

Research and Development at Fraunhofer CNT

The business areas of Fraunhofer CNT include the development of processes and materials as well as the physical and electrical characterization of high-performance-logics, derivates (e. g. embedded DRAM) and memory technologies for volatile and non-volatile devices.
In close cooperation with industrial partners and other R&D organizations, the objective of our institute is to develop innovative unit process solutions for nanoelectronic systems on 300 mm silicon wafers. The aim is to transfer research results fast into industrial manufacturing.

The range of services offered by Fraunhofer CNT is based on five competence areas:

- Analytics
- Functional Electronic Materials - Front End of Line
- Functional Electronic Materials - Back End of Line
- Devices & Integration
- Maskless Lithography

The competence areas do research especially in the following fields:

- Leading edge technology for nano-micro-electronic
- Enabling 300 mm production
- Nanostructuring

Ausstattung

Für das Fraunhofer CNT stehen derzeit 800 m² Reinraumfläche (Reinraumklasse 1000) sowie eine Infrastruktur zur Verfügung, die dem Industriestandard entspricht. Zusätzlich zu den ca. 40 Anlagen im Reinraum können umfangreiche Analyse- und Metrologieverfahren für die Forschung und Entwicklung sowie die Bausteincharakterisierung genutzt werden.
Die Einrichtung unterhält keine durchgängige Prozesslinie in der alle notwendigen Prozessschritte zur Realisierung höchstintegrierter Chips zur Verfügung stehen. Sie verfügt aber über neue, fertigungstypische Prozessgeräte, an denen die Partner zusammen mit den Wissenschaftlern im Fraunhofer CNT forschen und entwickeln können.

Teilprozessierte Wafer kommen von GLOBALFOUNDRIES - die innovativen Prozessschritte werden im Fraunhofer CNT durchgeführt. Die gewonnenen Erkenntnisse können dann sofort in die praktische Erprobung in der angrenzenden Fertigung übertragen werden. Dadurch lassen sich sowohl Investitionen für die Partner minimieren, als auch ein schnellerer Zeitablauf ermöglichen.

Environment

At present, Fraunhofer CNT uses 800 m² clean room area (class 1000) and an infrastructure which meets industry standards. In addition to 40 clean room tools, scientists at Fraunhofer CNT use considerable analytical and metrological processes for R&D as well as for the characterization of nanoelectronic devices.

The institute does not maintain a continuous process line to cover all the necessary process steps in order to realize high-integrated memory chips. However, Fraunhofer CNT possesses new process tools which are typical of production and enabling common research and development with its partners.

Pre-processed wafers are provided by GLOBALFOUNDRIES – innovative process steps will be operated at Fraunhofer CNT. Thus, the results can be transferred immediately into manufacturing. This enables partners to reduce their capital expenditures. Moreover, it allows a faster schedule.

PROFILE

COLLABORATION

Kooperationspartner in unmittelbarer Umgebung

Das Fraunhofer-Center Nanoelektronische Technologien - 2005 entsprechend dem Modell einer Public-Private-Partnership gegründet - ist neben der erfolgreichen Kooperation mit dem Halbleiterhersteller GLOBALFOUNDRIES Dresden Module One LLC & Co. KG auch für die Zusammenarbeit und Durchführung von Projekten mit verschiedenen Forschungseinrichtungen, Industriepartnern und Universitäten sowie Zulieferfirmen der IC-Industrie wie Material- und Geräteherstellern offen.

In unmittelbarer Umgebung des Fraunhofer CNT befinden sich die Halbleiterhersteller GLOBALFOUNDRIES, Infineon und X-Fab. Dazu bietet Dresden, eingebettet in Silicon Saxony, ausgezeichnete Standortbedingungen für das Fraunhofer CNT als etablierte Forschungsplattform der Nanoelektronik. Durch die lokale Nähe zu den Fertigungslinien des Partners und das vorhandene Know-how können viele Synergieeffekte genutzt werden. Dadurch ist es möglich, Entwicklungen und neue Prozesse schnell in die Fertigungsabläufe einzubauen, was es wiederum erlaubt Herstellungskosten und -zeit zu sparen.

„Durch die Nutzung von Synergien zwischen der Referenz von Fertigungslinien, basierend auf modernster 300 mm Wafertechnologie, sowie dem Fachwissen unserer Mitarbeiter können wir Projekte erfolgreich und zeitnah durchführen.“
Prof. Dr. Peter Kücher

Cooperation partner in the immediate vicinity

Fraunhofer Center Nanoelectronic Technologies was founded in 2005 according to the model of a public private partnership. A part from the successful cooperation with the semiconductor manufacturer GLOBALFOUNDRIES Dresden Module One LLC & Co. KG, the institute is open for the collaboration and execution of projects with different research organizations, industrial partners, universities as well as semiconductor suppliers such as material and tool manufacturers.

The semiconductor manufacturers GLOBALFOUNDRIES, Infineon and X-Fab are located close to Fraunhofer CNT. In addition, Dresden and Silicon Saxony offer excellent site conditions. Because of the proximity to the manufacturing lines of the partners and of the established know-how, Fraunhofer CNT benefits from numerous synergy effects. Thus, it is possible to implement innovative developments and new processes fast into manufacturing. It also enables the partners to save time and production costs.

„Benefiting from synergies between the reference of the manufacturing lines on the basis of latest 300 mm wafer technology as well as of the know-how of our employees, we are able to perform our projects successfully and immediately.“
Prof. Dr. Peter Kücher

FRAUNHOFER CNT IN FIGURES

Head of Administration: Antje Spitzer

Das Fraunhofer CNT erwirtschaftete 2011 einen Ertrag von ca. 8,8 Mio Euro. Der Betriebshaushalt setzte sich zu ca. 51 % aus Wirtschaftserträgen, zu etwa 7 % aus Erträgen aus nationalen öffentlichen Projekten, zu rund 3 % aus EU-Erträgen, zu rund 22 % aus sonstigen Erträgen und zu 17 % aus Sonderfinanzierungsmitteln zusammen.

Zur Bearbeitung der Forschungsaufträge stehen auf 800 m² Reinraumfläche und 200 m² Laborfläche modernste Laborausstattungen und Großgeräte zur Verfügung. Der Anlagenpark umfasst Abscheide- und Ätzanlagen für die Wärmebehandlung bei Hochtemperaturen sowie Inspektions- und Analysegeräte zum Bestimmen von Defekten und dem Messen von Schichteigenschaften.

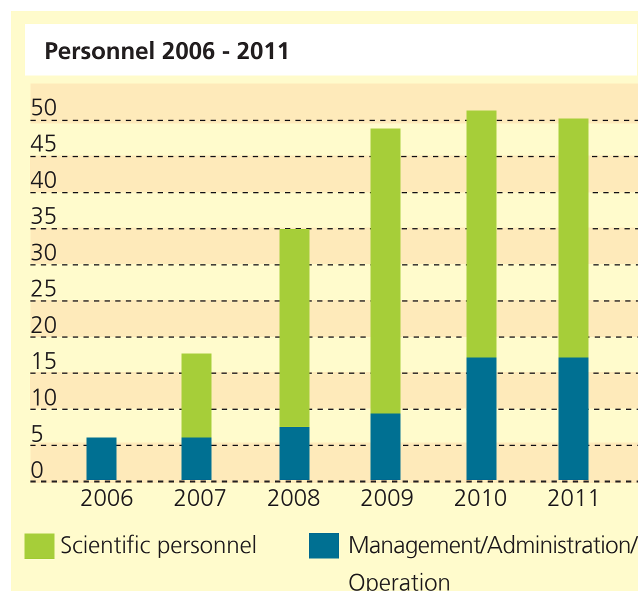
Zum Jahresende 2011 beschäftigte das Fraunhofer CNT 49 festangestellte Mitarbeiter. Das Personal setzte sich aus 32 Wissenschaftlern einschließlich 7 Doktoranden, 6 technischen Mitarbeitern und 11 Mitarbeitern in Management und Verwaltung zusammen. Mit modernstem Anlagenpark, intensiver Vorlaufforschung sowie einer langjährigen Industrieerfahrung stehen die Mitarbeiter des Fraunhofer CNT ihren nationalen und internationalen Kunden und Partnern zur Seite, um Innovationen für die Zukunft nutzbar zu machen.

Expenditures and Revenues 2011

Annual Budget 2011	in k €	in %
Revenues	**8.771**	
Industry	4.508	51,0
Publicity (national)	632	7,0
Publicity (EU)	281	3,0
Others	1.918	22,0
Additional Income	1.432	17,0

In 2011 Fraunhofer CNT generated revenues of about 8.8 million Euro. The operation budget was composed of 51 % of industry returns, 3 % earnings from national public projects, 7 % of EU earnings, 22 % of other revenues and 17 % of special financing.
In order to process R&D wafers professionally, Fraunhofer CNT has an area of 800 m² clean room and 200 m² laboratory available which are equipped with the latest semiconductor R&D tools. The equipment ranges from deposition and etching tools used for the heat treatment at high-temperatures as well as from inspection and analytic tools which are used for the characterization of defects and layers.

In the end of 2011, Fraunhofer CNT employed 49 permanent staff. The personnel was composed of 32 scientists including 7 Ph.D. students, 6 technicians and 11 employees in administration and management. Equipped with the latest devices, intense initial research and a long-lasting industry know-how, employees of Fraunhofer CNT provide support to their national and international customers and partners in order to realize innovations in the future.



Das Fraunhofer CNT hat 2011 ca. 1 Mio Euro investiert, um sein technisches Equipment zu erweitern. Diese Investitionen wurden aus dem Europäischen Fond für Regionale Entwicklung und vom Freistaat Sachsen gefördert sowie aus Sondermitteln finanziert.

Der strategische Industriepartner Globalfoundries setzte seine Zusammenarbeit mit dem Fraunhofer CNT kontinuierlich in mehrere bereits vor 2011 gestarteten Forschungsvorhaben fort.

Für Globalfoundries wurde so beispielsweise eine schädigungsfreie, plasmagestützte Strukturierung von Ultra-low-k Dielektrika für die Anwendung in einer sub30nm-Technologie entwickelt.
Ein weiteres Projekt beinhaltet die **Entwicklung zukünftiger High-k Gate-Dielektrik-Transistoren** einschließlich einer Machbarkeitsstudie für ferroelektrische Speicher.

Darüber hinaus arbeiteten die Wissenschaftler des CNT in einem Projekt an der **Entwicklung einer Verdrahtungstechnologie für kleinste Strukturen** unter Berücksichtigung der wachsenden Anforderungen an die elektrische Zuverlässigkeit, sowie in einem Projekt an der **Optimierung von Metal-Gate-Prozessen** für die Replacement-Gate-Technologie und Entwicklung von Prozessen zur Verbesserung der Zuverlässigkeit von High-k-Metal-Gate (HKMG)-Stapeln.

Das in 2010 von Globalfoundries beauftragte Projekt „Verbesserung der Mikroprozessoreneigenschaften mittels Einsatz von Kohlenstoff“ wurde in 2011 erfolgreich abgeschlossen.

Weitere Projekte wurden mit verschiedenen namhaften Forschungseinrichtungen und Unternehmen umgesetzt, so beispielsweise ein Projekt mit ASELTA Nanographics (Frankreich) zur E-Beam Proximity Effekt Korrektur für die Herstellung von optischen Masken und Anwendungen im Bereich der maskenlosen Lithografie.

The Fraunhofer CNT has invested about € 1 million to expand its technical equipment in 2011. These investments were financed through the European Regional Development Fund, the Free State of Saxony and from special funds.

The strategic industry partner Globalfoundries steadily continued his collaboration with the Fraunhofer CNT in several research projects that started before 2011.

One development for Globalfoundries was a damage-free, plasma-based patterning of ultra-low-k dielectrics for the use in a sub30nm technology. Another project involves the **development of future high-k gate dielectric transistors** including a feasibility study for ferroelectric memory.

Furthermore, scientists at CNT were working on a project to **develop a wiring technology for smallest structures**, considering the growing demands on the electrical reliability. Another project is working on the **optimization of metal-gate processes for the replacement-gate** technology and development of processes to improve the reliability of high-k metal gate (HKMG) stacks.

The in 2010 commissioned Globalfoundries project "Improvement of the microprocessor features through the use of carbon" was successfully completed in 2011.

Other projects have been implemented with several renowned research institutes and companies, such as the project with ASELTA Nano Graphics (France) for e-beam proximity effect correction for the manufacture of optical masks and applications in maskless lithography.

Entrance of Fraunhofer CNT

Zusammen mit der Namlab gGmbH entwickelte das Fraunhofer CNT **ALD-Abscheidetechniken** für Hafnumdioxid basierende neue Materialien und wenige atomlagendicke Schichtsysteme.

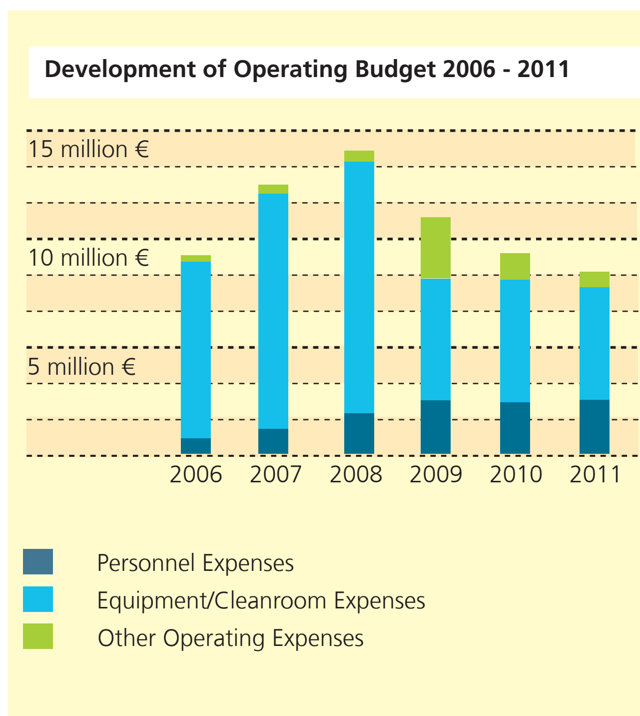
Im Rahmen des Spitzenclusters CoolSilicon ist das Fraunhofer CNT an dem Teilvorhaben „Technologien für energieeffiziente Computing-Plattformen" beteiligt und untersucht hier einen selektiven SiGe-Epitaxieprozess mit insiut-Dotierung.

Im Bereich Analytik erprobt das Fraunhofer CNT im Rahmen eines sächsischen Verbundprojektes gemeinsam mit der Firma X-FAB Silicon Foundries innovative Analyseverfahren für die Optimierung von Fertigungsprozessen bei der Herstellung von mikroelektronischen Bauelementen mittels 3D-Atomsonde, HR-TEM und SIMS.

Together with the NaMLab gGmbH, the Fraunhofer CNT developed **ALD deposition techniques** for Hafnumdioxid based new materials and a few atomic layer thick-layer systems.

As part of the Excellence Cluster "Cool Silicon" Fraunhofer CNT is involved in the sub-project "Technologies for Energy Efficient Computing Platforms" and is investigating a selective SiGe epitaxy with insiut doping.

As part of a joint Saxon project, Fraunhofer CNT and X-FAB Silicon Foundries testing innovative analytical methods for the optimization of manufacturing processes in the manufacture of microelectronic devices using 3D atom probe, HR-TEM and SIMS.



INNOVATION THROUGH COOPERATION

FRAUNHOFER-GESELLSCHAFT

Forschen für die Praxis ist die zentrale Aufgabe der Fraunhofer-Gesellschaft. Die 1949 gegründete Forschungsorganisation betreibt anwendungsorientierte Forschung zum Nutzen der Wirtschaft und zum Vorteil der Gesellschaft. Vertragspartner und Auftraggeber sind Industrie- und Dienstleistungsunternehmen sowie die öffentliche Hand.

Die Fraunhofer-Gesellschaft betreibt in Deutschland derzeit mehr als 80 Forschungseinrichtungen, davon 60 Institute. Mehr als 17.000 Mitarbeiterinnen und Mitarbeiter, überwiegend mit natur- oder ingenieurwissenschaftlicher Ausbildung, bearbeiten das jährliche Forschungsvolumen von 1,7 Mrd Euro. Davon fallen 1,4 Mrd Euro auf den Leistungsbereich Vertragsforschung. Zwei Drittel dieses Leistungsbereichs erwirtschaftet die Fraunhofer-Gesellschaft mit Aufträgen aus der Industrie und mit öffentlich finanzierten Forschungsprojekten. Nur etwas ein Drittel wird von Bund und Ländern als Grundfinanzierung beigesteuert, damit die Institute Problemlösungen erarbeiten können, die erst in fünf oder zehn Jahren für Wirtschaft und Gesellschaft aktuell werden.

FRAUNHOFER IN DRESDEN: GEBALLTE FORSCHUNG

Die Fraunhofer-Gesellschaft ist mit sechs Instituten und sechs weiteren Einrichtungen in Dresden vertreten. Die zwölf Fraunhofer-Einrichtungen beschäftigen zusammen mehr als 1.100 Mitarbeiter bei einem jährlichen Umsatz von über 100 Mio Euro. Für die nächsten Jahre wird ein weiteres Wachstum prognostiziert.

Neben der außerordentlich hohen Dichte an Forschungseinrichtungen zeichnet sich der Standort Dresden durch eine enge Verflechtung von Industrie und Forschung aus. Die daraus entstehenden Spitzenleistungen und innovativen Entwicklungen setzen weltweite Impulse.

FRAUNHOFER-GESELLSCHAFT

Research for practice is the main issue of all activities pursued by the Fraunhofer-Gesellschaft. The research organization, which was founded in 1949, undertakes applied research that drives economic development and serves the wider benefit of society. Its services are solicited by customers and contractual partners in industry, the service sector and public administration.

At present, the Fraunhofer-Gesellschaft maintains more than 80 research units in Germany, including 60 Fraunhofer institutes. The majority of the more than 17.000 employees are qualified scientists and engineers who work with an annual research budget of 1.7 billion euro. More than 1.4 billion euro of this amount are generated through contract research. Two thirds of the Fraunhofer-Gesellschaft's contract research revenues derive from contracts with industrial partners and from publicly financed research projects. Only one third is contributed by the German federal and Länder governments in the form of base funding which enables the institutes to work ahead on solutions to problems that will become relevant to industry and society in five or ten years.

FRAUNHOFER IN DRESDEN: CLUSTERED RESEARCH

The Fraunhofer-Gesellschaft is represented in Dresden by six institutes and six other facilities. More than 1.100 employees work for the twelve Fraunhofer facilities. The annual turnover amounts to more than 100 million euro and further growth is expected within the next years.

In addition to the extraordinarily high density of research facilities, the region is characterized by the close connection between research and industry, resulting in the creation of leading-edge services and innovative developments which have a global impact.

FRAUNHOFER VERBUND MIKROELEKTRONIK

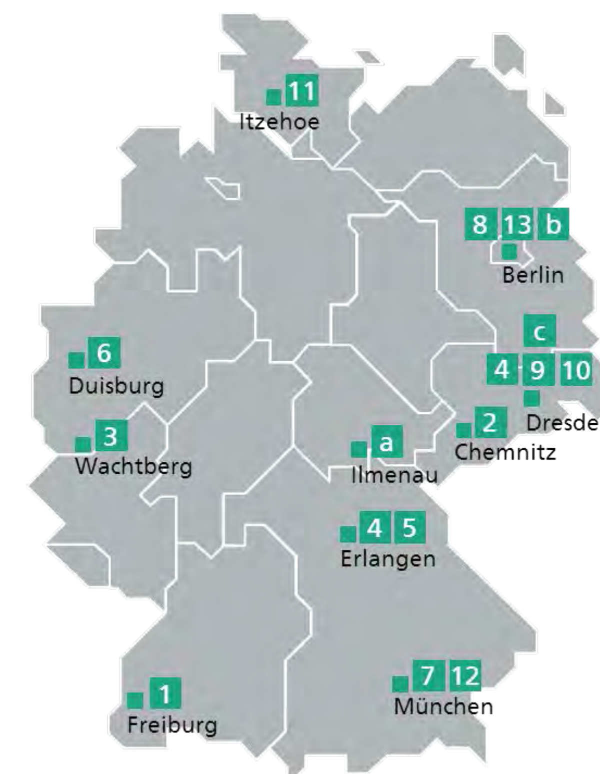
Der Fraunhofer-Verbund Mikroelektronik (VμE) koordiniert die Aktivitäten der auf den Gebieten Mikroelektronik und Mikrointegration tätigen Fraunhofer-Institute.

Die Technologiekompetenz des Verbunds reicht von der klassischen CMOS-Technologie bis zum Einsatz innovativer Systemlösungen. Sie schließt neben Silizium auch Verbindungshalbleiter und neue Materialien ein. Die Kompetenz in der Entwicklung von CMOS- und anderen Bauelementetechnologien für die Mikroelektronik stellt die Basis sowohl für technologische Dienstleistungen als auch für anwendungsbezogene Komponentenentwicklung dar. Das Fraunhofer CNT ist Ansprechpartner für die Bereiche „More Moore" und „Beyond CMOS" im Geschäftsfeld Technologie.

FRAUNHOFER GROUP MICROELECTRONICS

The Fraunhofer Group for Microelectronics (VμE) coordinates the activities of Fraunhofer institutes working in the fields of microelectronics and microintegration.

The group's expertise ranges from classic CMOS technology to the use of innovative system solutions. Apart from silicon, this also includes compound semiconductors and new materials. Expertise in developing CMOS and other device technologies for microelectronics forms the basis for both, technological services and application-specific component development. Fraunhofer CNT is the contact for the business area Technology which consists of two divisions: „More Moore" and „Beyond CMOS".



1 Angewandte Festkörperphysik IAF
2 Elektronische Nanosysteme ENAS
3 Hochfrequenzphysik und Radartechnik FHR
4 Integrierte Schaltungen IIS
5 Integrierte Systeme und Bauelementetechnologie IISB
6 Mikroelektronische Schaltungen und Systeme IMS
7 Modulare Festkörper-Technologien EMFT
8 Nachrichtentechnik, Heinrich-Hertz-Institut HHI
9 Nanoelektronische Technologien CNT
10 Photonische Mikrosysteme IPMS
11 Siliziumtechnologie ISIT
12 Systeme der Kommunikationstechnik ESK
13 Zuverlässigkeit und Mikrointegration IZM

Gastinstitute / Guest Institutes
a Digitale Medientechnologie IDMT
b Offene Kommunikationssysteme FOKUS
c Zerstörungsfreie Prüfverfahren IZFP

INNOVATION THROUGH COOPERATION

CLUSTER NANOANALYTIK

Seit Oktober 2009 ist das Fraunhofer CNT Mitglied im Dresdner Fraunhofer-Cluster Nanoanalytik. Zehn Fraunhofer-Institute und drei Fakultäten der Technischen Universität Dresden sowie das Helmholtz-Zentrum Berlin bündeln ihre Kompetenzen und decken das gesamte Themenspektrum der Nanoanalytik ab. Die Institute sind flexibel vernetzt und werden auch sehr umfassenden Anforderungen im Bereich Analytik gerecht.

ALD LAB DRESDEN

Im Oktober 2010 wurde das ALD Lab Dresden gegründet. Mit dem Lab werden Kompetenzen auf dem Gebiet der ALD (Atomlagenabscheidung) am Standort Dresden, dem Institut für Halbleiter- und Mikrosystemtechnik (IHM) der Technischen Universität Dresden (Prof. Johann Bartha) und der ALD-Gruppe des Fraunhofer CNT (Dr. Jonas Sundqvist) zusammengeführt. Gemeinsam entwickeln die Partner neue ALD-Precursoren und –Prozesse für die Halbleiter- und Photovoltaik-Industrie.

E-BEAM-INITIATIVE

Seit April 2010 ist das Fraunhofer CNT offizielles Mitglied der E-Beam-Initiative.
Die Initiative bietet ein Forum für bildungs- und verkaufsfördernde Aktivitäten, unter dem Gesichtspunkt eines neuen „design-to-manufacturing"-Ansatzes, bekannt als „design for e-beam" (DFEB). DFEB reduziert Maskenkosten für Halbleiterbauelemente, in Verbindung mit Design, Design-Software, Herstellung, Herstellungsmaterialien und Hersteller-Software-Expertise.

CLUSTER NANOANALYTIK

Since October 2009, Fraunhofer CNT has been a member of the Fraunhofer-Cluster Nanoanalytics in Dresden. Ten Fraunhofer institutes, three faculties of the Dresden University of Technology as well as the Helmholtz-Zentrum Berlin consolidate their competences and thus cover the entire field of nanoanalytics. The institutes are flexibly linked and can meet comprehensive analytics requirements.

ALD LAB DRESDEN

The ALD Lab Dresden was founded in October 2010. It is a joint venture of the Institut für Halbleiter- und Mikrosystemtechnik (IHM) of the Dresden University of Technology (Prof. Johann Bartha) and the ALD group of Fraunhofer CNT (Dr. Jonas Sundqvist) which combines their competences in the field of ALD (atomic layer deposition). The workscope is to develop new ALD precursors and processes for the semiconductor and photovoltaic industry.

E-BEAM INITIATIVE

Since April 2010, Fraunhofer CNT is an official member of the e-beam initiative.
The initiative provides a forum for educational and promotional activities considering a new "design-to-manufacturing" approach known as "design for e-beam" (DFEB). DFEB reduces mask costs for semiconductor components linked to designs, design software, manufacturing, manufacturing materials and manufacturer's software expertise.

COMPETENCE AREAS AND RESEARCH RESULTS

Microelectronics is the basic technology for a lot of technical applications. The progress in the automobile and the computer industry can be owned by this technology. Microelectronic systems have to become smaller and smaller and more energy efficient. They also have to provide much more power and combine more and more new features. The key activities of Fraunhofer CNT focus on the development of innovative processes for high-performance transistors as well as the development of nanoelectronic integrated circuits to fulfill the tasks mentioned above. Fraunhofer CNT divides its groups into five areas of competences.

ANALYTICS

FUNCTIONAL ELECTRONIC MATERIALS FRONT-END OF LINE

FUNCTIONAL ELECTRONIC MATERIALS BACK-END OF LINE

MASKLESS LITHOGRAPHY

DEVICES & INTEGRATION

COMPETENCE AREA ANALYTICS

Group Manager
Analytics

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COMPETENCES

The competence area Analytics concentrates on the characterization of materials needed for the fabrication of modern semiconductor chips. It focuses on topics such as the distribution and activity of dopants, properties of surfaces and interfaces, crystallization and phase formation, lateral resolved stress measurements and quantification of impurities. In order to meet the challenges of ongoing miniaturization, we engage in the improvement of existing methods and also in the application of new methods, e. g. atom probe tomography.

TRENDS

In 2011 Fraunhofer CNT continued its work on atom probe tomography (APT) in co-operation with external partners from the industry and academic research institutions.
Together with our local academic partners from the Helmholtz -Zentrum Dresden-Rossendorf, the TU Dresden and the Leibniz-Institute for Solid State and Materials Research Dresden we successfully established the Advanced Atom Probe Lab and studied a wide range of materials like metallic glasses ,ODS hardened steels or pnictide based superconducting thin films.

Together with our industrial partners from GLOBALFOUNDRIES and X-Fab we are have been working on the characterization of ultrathin oxide based films used in high-K metal gate stack for high performance transistors and SONOS (Silicon-Oxide-Nitride-Oxide-Silicon) based non-volatile memories in the framework of two publically funded projects.
Finally, a number of smaller projects have been carried out in co-operation with several partners from industrial and academic institutions that included amongst others the characterization of gallium-arsenide based materials for optical applications and materials for solar applications.

ATOM PROBE TOMOGRAPHY

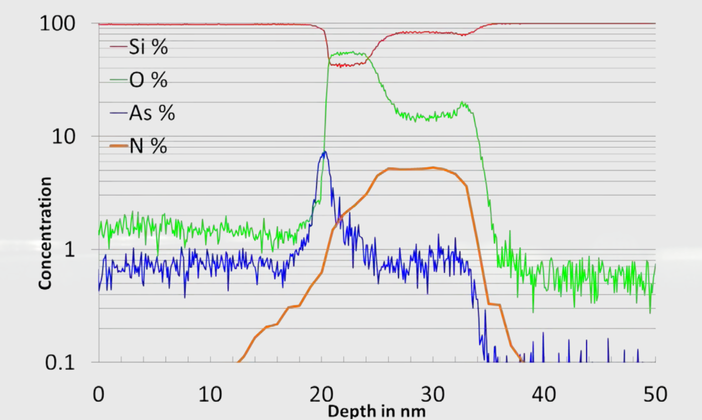
SONOS stacks for non-volatile memory applications

We have used APT to analyze SONOS (Silicon-Oxide-Nitride-Oxide-Silicon) based non-volatile memory cells within the publically funded project CoolAnalytics, which started in April 2011. The project aims to understand the influence of the distribution of elements within the charge trapping layer on the relevant electrical properties like charge retention, reliability and programming voltage in order to optimize the manufacturing process.
As the non-volatile memory cells under investigation are two-dimensional structures and we are eventually interested to determine the concentration of silicon, nitrogen and oxygen in two dimensions as well, we need an analysis method that provides high spatial resolution and a good sensitivity. APT is the most promising method for extracting these kind of information. The major difficulty in these analyses is the mass overlap of Si^{2+} and N^{+} at mass 14 and Si^{+} and N_2^{+} at mass 28 respectively. We have to refer to statistical methods that separate the elements based on their isotopic distribution in order to solve this challenge.

Initial APT results from gate stacks for SONOS devices are shown in Fig. 1 and Fig. 2. Fig. 1 demonstrates that we can analyze the stack of isolating materials with APT and clearly resolve each layer. As isolating layers are notoriously difficult to analyze this is a major step in the project. The depth profile in Fig. 1 shows the thick top oxide, the thin bottom oxide and the intermediate oxy-nitride containing 5% nitrogen. Unfortunately, the oxygen quantification in the SiO_2 layers do not show the expected 66% oxygen. This result is likely to be caused by a combination out-gassing of oxygen during the analysis and reconstruction artifacts. . The analysis however reveals a diffusion of nitrogen into the top oxide and a strong accumulation of arsenic at the interface between the Poly-Si electrode and the top oxide layer. Additionally, arsenic is enriched at grain boundaries in the Poly-Si covering the gate stack (Fig. 2).

Precipitation hardened steels

The hardening of steel by the precipitation of nano-scaled particles is a common method in steel metallurgy. APT is an ideal method to study these precipitation phenomena in detail. Together with Fraunhofer IWS (Dr. Jörg Kaspar and Dr. Jörg Bretschneider) we have investigated the martensitic stainless steel X5CrNiCuNb 16-4 hardened by Cu precipitates formed during a two-step aging process.
APT reveals the elemental composition, size, distribution and density of the Cu precipitates. The size of the precipitates was in the range of 2-6 nm diameter. The precipitate density was found to be 0.0015 nm^{-3}, which means, that one precipitate can be found within a cube of approximately 8.7 nm length.



1 *Depth profile of a SONOS layer stack showing the distribution of the main constituents.*

ANALYTICS

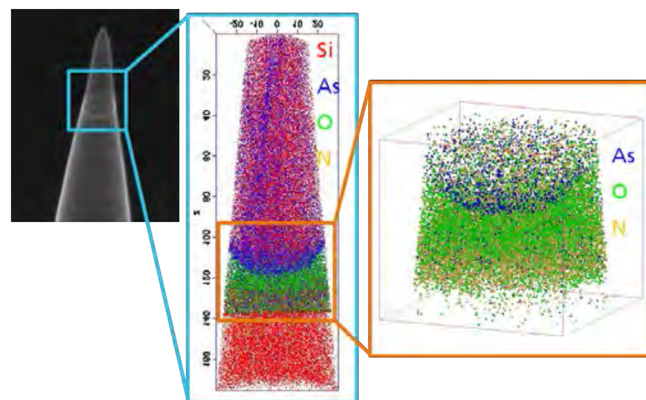
The results clearly show, that the precipitates are enriched in Cu and Ni whereas Fe and Cr are depleted compared to the matrix composition. The vicinity of the precipitates is depleted in Cu (Cu diffusion zone). A concentration profile for constituent elements as calculated from averaging over 300 precipitates is shown in Fig 3. The 3D spatial distribution of Cu precipitates in the matrix is shown in Fig. 4. Furthermore, the spatial distribution micrograph obtained using atom probe tomography reveals, that carbon is enriched at an arch-like grain boundary (Fig. 5).

Superconducting thin films

In 2008 a new class of high-temperature superconductors has been discovered in layered iron arsenic compounds. They are extreme type II superconductors (similar to the cuprates) of multiband nature (similar to MgB_2). Since their discovery thin films of the intermetallic cobalt-doped $BaFe_2As_2$ (Ba-122) phase were synthesized by pulsed laser deposition. The epitaxial growth of this compound on bcc iron offers the possibility to grow $Fe/Ba(Fe_{1-x}Co_x)_2As_2$ multilayers that possess magnetically influenced superconducting and transport properties. This layer stack has been analysed by APT in co-operation with Dr. Silvia Haindl and Jan Engelmann from IFW Dresden.

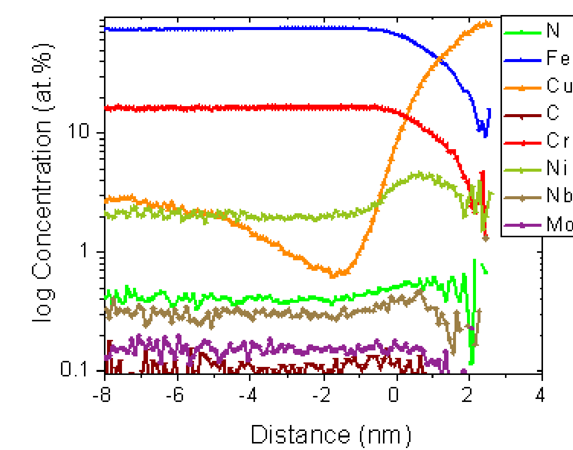
In order to fabricate such multilayers for electronic applications like Josephson junctions a detailed understanding of its microstructure is needed. The investigated multilayer was grown by pulsed laser deposition under ultrahigh vacuum conditions on $MgAl_2O_4$ substrates. First, an iron buffer layer was deposited at room temperature and subsequently heated up to 700°C to achieve a closed iron layer with smooth interfaces. The Ba-122 layer was grown at the same temperature. After cooling down to room temperature an approximately 5 nm thick iron interlayer was deposited and again heated up. Finally, a second Ba-122 layer was deposited at 700 °C. Epitaxial film growth was confirmed by X-ray analysis. The Fe/Ba-122 stack is superconducting up to a temperature of 22K.

APT results show small scale inhomogeneities of the barium, iron, arsenic, and cobalt distribution in the Ba-122 film (Fig. 6). The analysed samples revealed a Co dopant gradient along the film thickness as well as Ba- and Fe-rich regions. The oxygen contamination was found to be strongest on the Fe layers.

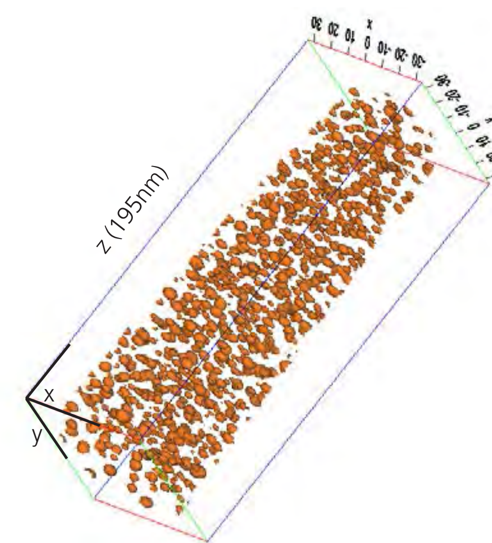


2 *SEM image of a ready-to-run tip including the ROI (left) and 2d projection of 3D atomic maps of the SONOS stack (middle and right) showing enrichment of arsenic at the grain boundaries and at the top oxide.*

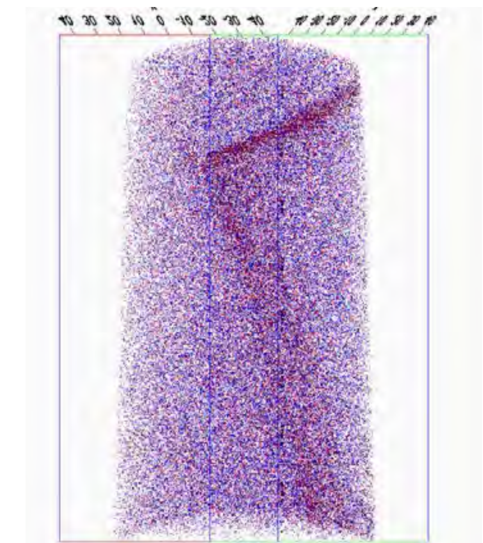
Matrix | Cu diffusion zone | Cu ppt



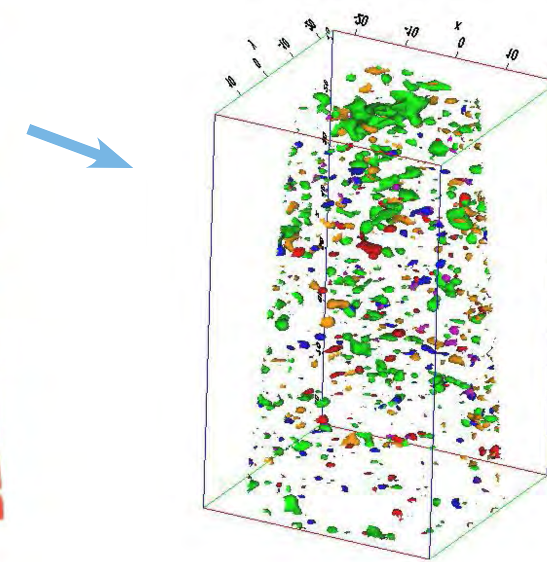
3 *Concentration profile calculated from a proximity histogram averaged over 300 precipitates*



4 *3D spatial distributions of the Cu precipitates in the steel matrix*

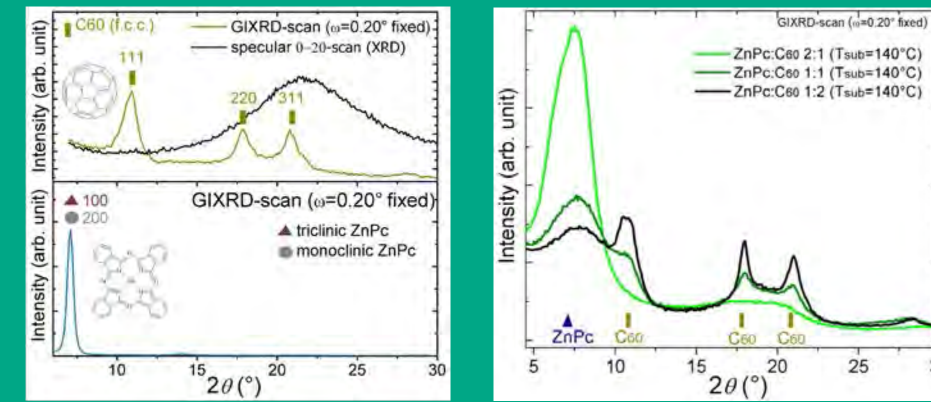


5 *Carbon enrichment at an arch-like grain boundary*



6 *Distribution of the iron concentration in the layer stack (left side) and iso-concentration surfaces of iron, arsenic, cobalt, barium and oxygen showing inhomogeneities in the Ba-122 layer*

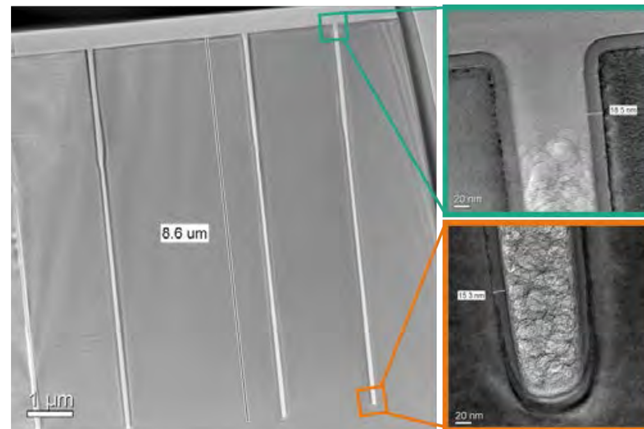
ANALYTICS



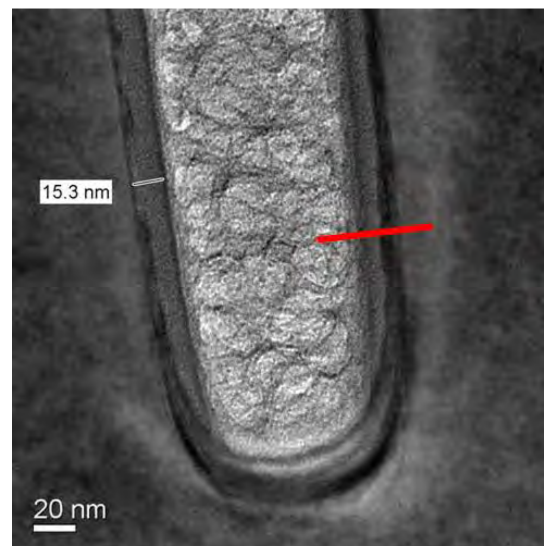
9 *GIXRD scans of pristine C60 and ZnPc films (left)*
GIXRD scans of heated blend layers with different ZnPc:C60 ratio (right)

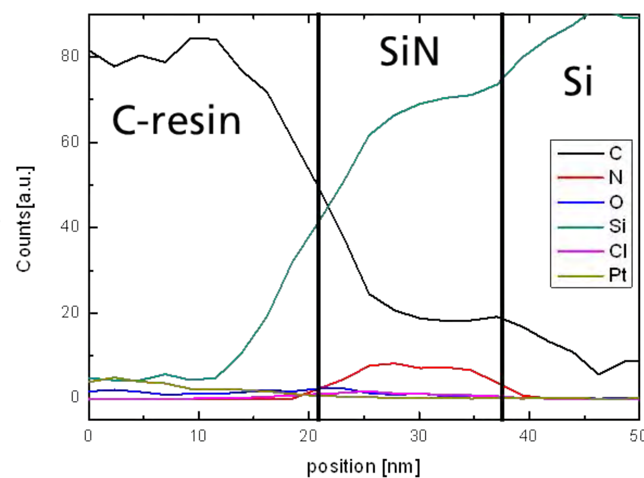
TRANSMISSION ELECTRON MICROSCOPY

At Fraunhofer CNT, the ALD process development and the evaluation of new ALD precursors for the deposition of dielectrics is one of the core competences. TEM investigations of the step coverage of a new precursor for the deposition of Si_3N_4 into a test structure with high-aspect ratio trenches have been carried out to support these activities. In order to reduce preparation artefacts during FIB preparation, the trenches were filled by a special resin, which shows the grainy structure in the high resolution images (Fig. 7 & 8). The ALD deposited Si_3N_4 appears in middle gray. The analysis of the layer thickness at the top and at the bottom shows excellent step coverage of better than 80% (Fig. 7). A EDX line scan over the Si3N4 layer reveals, that the Si_3N_4 layer is oxidized at the surface (Fig. 8).



7 *Analysis of the step coverage of an ALD grown Si3N4 layer by TEM (left side: overview image; right side: top and bottom details)*





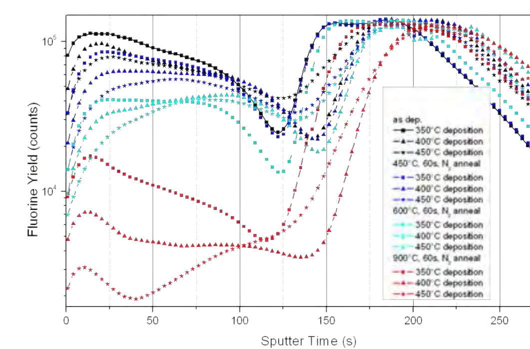
8 *EDX line scan over ALD grown Si3N4 layer (left side: red bar shows position of EDX scan; right side: EDX results)*

X-RAY DIFFRACTION

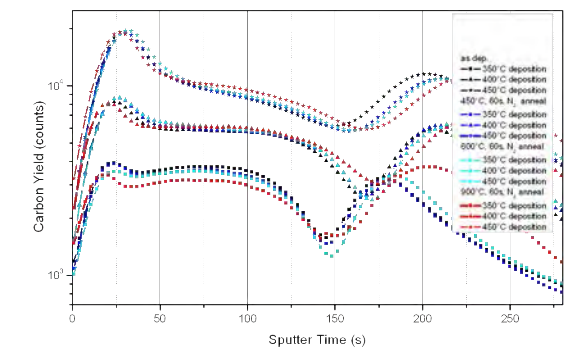
We continued with our successful co-operation on the characterization of organic thin films with Christoph Schünemann and Chris Elschner from TU Dresden, Institute for Applied Photophysics (IAPP). These films have potential applications in the field of organic electronics. Especially, we focused on the influence of the deposition temperature and the mixing ratio on the phase separation and layer morphology in blend layers of C60 and Zinc-phtalocyanide (ZnPc) which may be used as photoactive layer in organic solar cells. Due to the low layer thickness of 150nm or less, the measurements need to be carried out in grazing incidence geometry. A comparison to standard Bragg-Brentano geometry is shown in Fig. 9. While in the grazing incidence mode the reflections from the C60 film are clearly visible, in specular Bragg-Brentano geometry only the broad hump from the glass substrate is visible. Both molecules have a different shape, as shown in the inset of Fig. 9a, leading to the formation of separated C60 and ZnPc domains. Enhanced phase separation was observed for higher C60 contents and for higher growth temperatures resulting in improved charge carrier percolation paths and therefore improved solar cell performance. The GIXRD measurement clearly indicates that even for high ZnPc content within the blend, ZnPc is not able to crystallize, even for elevated substrate temperatures of 140°C (Fig. 9).

TOF-SIMS

The deposition of 5 nm thin TaCN films from tetramethyldisilazane (TDMS) and TaF5 precursors on Si substrate by an ALD process was studied by ToF-SIMS measurements. These films are used as etch stop layers in the replacement gate technology for the sub-28 nm node. The ToF-SIMS measurements are performed to determine the influence of the deposition temperature and the temperature of a subsequent post deposition anneal (PDA) on the carbon and fluorine concentration within the film. From the measurements it is obvious, that the PDA temperature has a significantly higher influence on the fluorine contamination within the film than the deposition temperature (Fig. 10). The decreasing fluorine concentration upon higher PDA temperature can be attributed to outgassing of fluorine. Otherwise, the carbon content is almost independent of the PDA temperature but shows a significant dependence on the deposition temperature as shown in Fig. 11. The N/C ratio (N not shown here) increases with increasing temperature of deposition due to the growth behavior of the ALD precursors.



10 *Depth profile of the fluorine intensity in dependence of PDA and deposition temperature*



11 *Depth profile of the carbon intensity in dependence of PDA and deposition temperature*

FUNCTIONAL ELECTRONIC MATERIALS FRONT-END OF LINE

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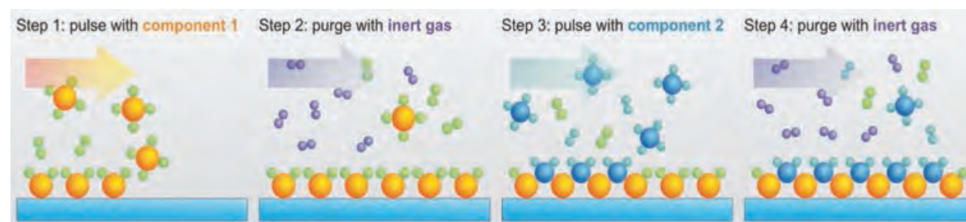
COMPETENCES

Objective of this research area is the development of insulating, semi-insulating and conductive thin films. These materials are suitable for various applications in micro- and nanoelectronics. One of the core competencies of the group is the Atomic Layer Deposition (ALD) of dielectric and conductive layers on 300 mm silicon wafers. The broad spectrum of ALD research activities covers different technical areas: ALD precursor testing, hardware and equipment evaluation as well as material and process development for high-volume manufacturing. Fraunhofer CNT works in close collaboration with industrial and academic partners. Hence, the Dresden ALD community established the „ALD Lab Dresden" as a common platform in fall 2010.

TRENDS

The focus of our R&D activities are high-k/metal gate (HKMG) stacks for coming generations of field effect transistors (FET) and high-k dielectrics and electrodes for non-volatile memories (NVM) and MIM-based capacitors.In the field of ferroelectric memories (FeFET) Fraunhofer CNT made a significant contribution through the engineering of ferroelectric hafnium oxide (HfO_2) creating the "most aggressively scaled" FeFETs using ferroelectric Si:HfO_2 in a 28 nm HKMG stack (TiN/Si:HfO2/SiO_2/Si). Fully functional FeFETs could be fabricated fulfilling current Flash specification in terms of data retention and endurance, but with much lower power consumption and DRAM-like write/erase speed. MIM capacitors are used in stand-alone and embedded DRAM and as integrated passive devices for RFCMOS. In 2011, we optimized the interfaces in the MIM stack to further improve the linearity of the TiN/ZrO_2-based capacitors. In addition, we developed a low cost tantalum carbo nitride (TaCN) ALD process on a large batch furnace. Beside the usage in the Replacement Gate transistor technology this process can be used also for memory applications in high-volume manufacturing (e.g. MONOS Flash) and heater electrodes for phase change memory (PCRAM).



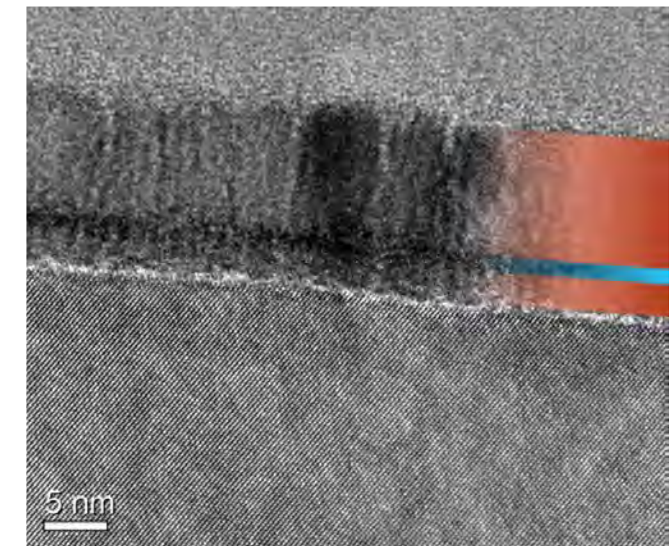
1 *The ALD cycle of a metal oxide deposition is composed of the following steps: metal-containing precursor pulse (step 1), purge of non-reacted precursor and reaction products with inert gas (step 2), oxidant pulse e.g. ozone or water (step 3) and a second inert gas purge to remove reaction products (step 4). The sequence is repeated several times to achieve the desired film thickness.*

METAL NITRIDES

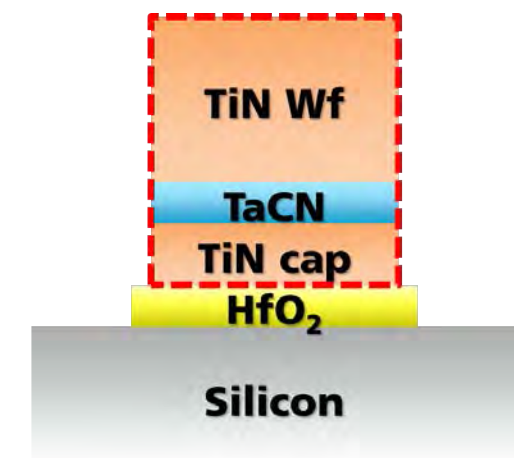
Since its release in the early 1950's the transistor has undergone a continuous scaling process. The recent problem of leakage current through the ever shrinking silicon dioxide gate dielectric was tackled with the introduction of new high-k dielectric materials such as hafnium dioxide together with metal gate electrode materials such as metal nitrides.
Using the Replacement Gate technology, metal nitrides are deposited by ALD, as the small feature sizes require conformal film growth. For further structuring of pFET and nFET, an etch stop layer is required within the metal gate film stack.

The deposition of a tantalum nitride based etch stop layer and diffusion barrier via 300 mm batch furnace ALD was developed at Fraunhofer CNT. The film showed a high growth rate and very conformal growth with very little surface roughness. Thorough material characterization confirmed etch-stop and diffusion barrier properties of the deposited TaCN films, as required for film in the Replacement Gate process flow.

Together with the process of titanium nitride ALD, a batch furnace in-situ process was then developed for the deposition of a complete TiN-TaN-TiN metal gate stack for the integration into the replacement gate process flow. The in-situ deposition enables well controlled interface treatments in between the metal films, as well as a low cost of ownership due to the high throughput of the batch furnace. This ALD process enables further transistor scaling below the 28 nm node for future Replacement Gate applications.



2 *HRTEM of a TiN-TaCN-TiN metal gate film stack deposited in-situ via ALD on the ASM A412 large batch furnace (red: TiN, blue: TaN).*



3 *Replacement Gate Stack schematic: TiN Wf - workfunction layer to control gate work function, TaCN - etch-stop and diffusion-barrier layer, TiN cap - capping layer to control interface to gate dielectric*

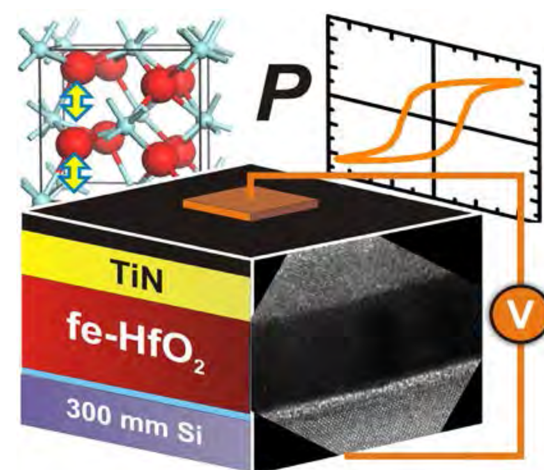
FUNCTIONAL ELECTRONIC MATERIALS - FRONT-END OF LINE

FERROELECTRIC FIELD EFFECT TRANSISTORS FOR FUTURE MEMORIES

Microelectronics and data storage technologies in particular, are strongly dependent on the ever-progressing strive to smaller feature sizes. Only then the cost savings in mass production are achieved necessary to remain competitive in a market of rapidly increasing storage density. Thus, in analogy to the aggressive scaling of logic transistors, the device density per unit area of the high-volume segments SRAM, DRAM and FLASH continuously increases with each new technology introduced. Nevertheless, despite their high scalability those conventional technologies are in many aspects inferior to new, innovative store concepts. The diversification of storage applications (mobility, cloud computing, long term storage, etc.) makes room for new storage technologies, generally summarized as "emerging memories".

The individual combination of memory properties with respect to nonvolatility, speed, power consumption, endurance and scalability gives concepts such as STT-MRAM(magnetic RAM), RRAM(resistive RAM), PCRAM(phase change RAM) and FRAM (ferroelectric RAM) a clear edge over the aforementioned mass memories. However, regarding power consumption during switching operation the FRAM, even in the field of emerging memories, has to be accentuated. Especially in the case of 1T FRAM (ferroelectric field effect transistor FeFET) the switching process is limited to a simple field-effect whose power consumption in relation to the current-driven switching in the STT-MRAM, RRAM and PCRAM has a vanishingly low energy consumption.

The successful integration of such an energy-efficient storage device into industrial production, however, had been considerably more difficult than expected and was limited by the available of integrated ferroelectric materials. Already known ferroelectrics such as lead-zirconat-titanate (PZT) or strontium-bismut-tantalate (SBT) lack back end of line (BEOL) stability, full CMOS compatibility and suffer from a high

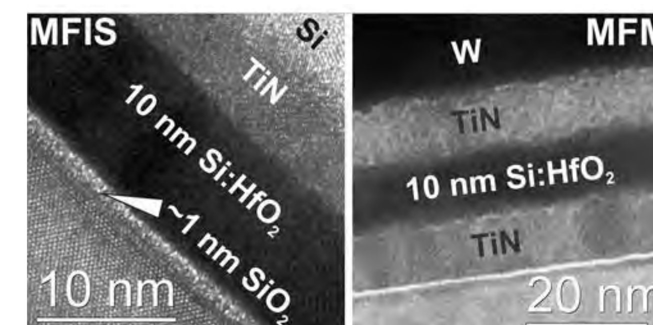


1 *Conventionalized gate structure of a HfO2-based ferroelectric field effect transistor.*

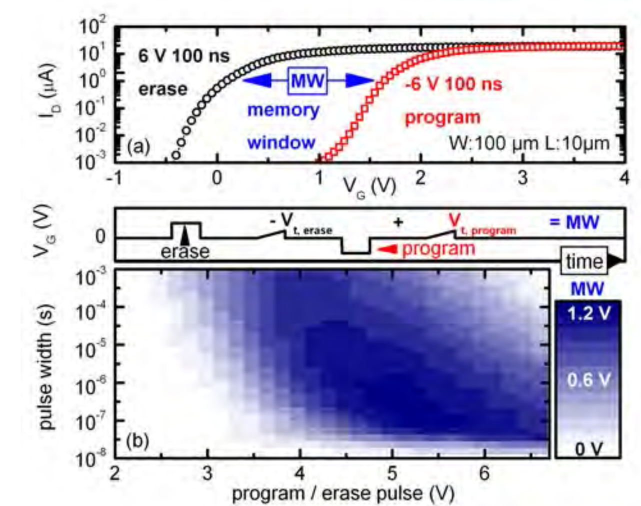
physical-layer thickness (low coercive fields, high dielectric constant) that only with considerable effort can be integrated into a conventional process flow. However, with the successful stabilization of ferroelectricity in HfO_2, a material system already well-known to microelectronic engineering, a new approach and therewith a new perspective for highly scaled, ferroelectric memories has been demonstrated. Scientist of the Fraunhofer CNT have identified several strategies to form ferroelectric HfO_2 and in the course of the projects MERLIN and HEIKO developed large expertise in depositing, structuring and characterizing those novel ferroelectric materials.

Currently the integration of an actual memory device based on an HfO_2 based ferroelectric field effect transistor has reached a final stage. In cooperation with our long term partners GLOBALFOUNDRIES and Namlab gGmbH fully functional ferroelectric field effect transistors on a state of the art 28 nm ground rule have been demonstrated.

Figure 2 depicts TEM cross sections of the gate stack of an earlier but comparable ferroelectric device, as well as a ferroelectric MIM capacitor used for process qualification and ferroelectric parameter extraction. Basic device operation was statistically verified and is representatively depicted in Figure 3a. Endurance comparable to current Flash technologies as well as data retention exceeding 10 years was further demonstrated. Additionally, outstanding switching times below 20 ns were achieved as can be seen in the time and field dependent memory window matrix in Figure 3b. In summary this predicts a fast, highly scaled, non-volatile memory concept based on a highly engineered, ferroelectric HfO_2. In current and future



2 *TEM cross section of a HfO2-based ferrolectric field effect transistor and a metal-ferroelectric-metal capacitor.*



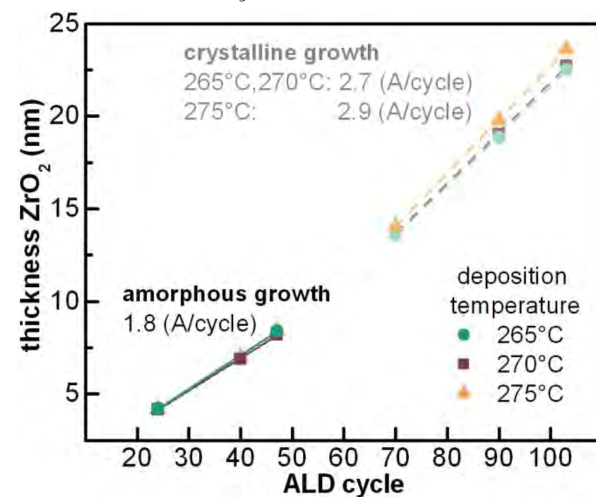
3 *Basic device operation of a ferroelectric field effect transistor (a). Time and field dependence of ferroelectric switching and its impact on memory window evolution.*

projects a 100 bit demonstrator will be fabricated representing the final step in putting the newly discovered ferroelectric properties of HfO_2 to a useful application in industrial scale.

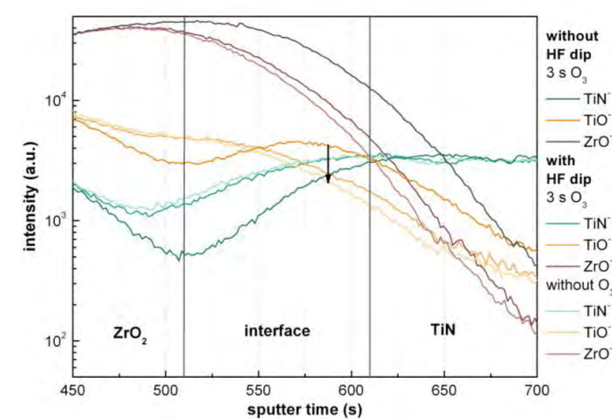
FUNCTIONAL ELECTRONIC MATERIALS - FRONT-END OF LINE

HIGH-K MATERIALS FOR MIM CAPACITORS

ZrO_2 is of very high interest in semiconductor industry mainly as high-k dielectric in DRAM, eDRAM or even resistive RAM. Above all, no alternative materials are in sight for the next generations of DRAM. Thus, further improving of deposition processes, of material properties and of integration schemes is essential to meet the strict requirements of future devices. One key challenge is reducing the process time of the bottle neck high-k ALD deposition. The most common process used for ZrO_2 deposition is TEMAZ/O_3 with a published growth rate of 1 Å/cycle. Thereby, the O_3 process causes oxidation of the TiN bottom electrodes resulting in MIM capacitor asymmetries and capacitance linearity issues. At the Fraunhofer CNT, we improved the TEMAZ/O_3 ALD process and studied the growth and crystallization behavior of thin ZrO_2 films. A growth rate of 1.8 Å/cycle up to 2.7 Å/cycle could be achieved by increasing the TEMAZ and the O_3 pulse times (Figure 1). Linear growth and good uniformity on 300 mm wafers could be proved for an ALD window up to 270 °C which is comparable to published TEMAZ/O_3 processes. The increase of the growth rate correlates to the crystallization of the ZrO_2 films during deposition starting at a critical film thickness. Besides the fast growth rate the deposited ZrO_2 layers show very good electrical performance with a CET of 0.7 nm and a leakage current of $2.6 \cdot 10^{-9}$ A/cm² at -1 V for a 7 nm thick crystalline film. Additionally, the new ZrO_2 ALD process was used to optimize the integration scheme of MIM capacitors with TiN electrodes addressing the bottom interface between ZrO_2 and TiN. In a first step, the TiN surface was studied in detail after an HF-Dip by XPS and Rs measurements to implement a time coupling between TiN and ZrO_2 deposition. Interestingly, the native TiO_2 can be reduced but never removed completely. In a second step, the influence of the O_3 oxidation was minimized by several process variations including lower O_3 pulse times or skipping the O_3 pulse only for the first cycles of the ALD deposition. AR-XPS and ToF-SIMS depth profiles show a significant decrease of the TiO_2 between ZrO_2 and TiN by using an HF-Dip. This reduction is intensified by the ZrO_2 process without O_3 which is visible by the decrease of the TiO-ion at the interface between ZrO_2 and TiN in Figure 2.



1 *Linear growth of ZrO_2 from a new TEMAZ/O_3 process at different deposition temperatures.*



2 *ToF-SIMS depth profile of the interface between ZrO2 and TiN after different interface treatements.*

cleanroom at Fraunhofer CNT

FUNCTIONAL ELECTRONIC MATERIALS - BACK-END OF LINE

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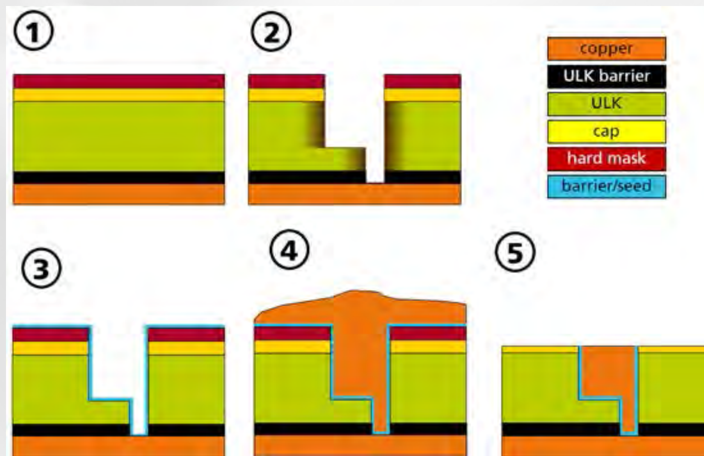
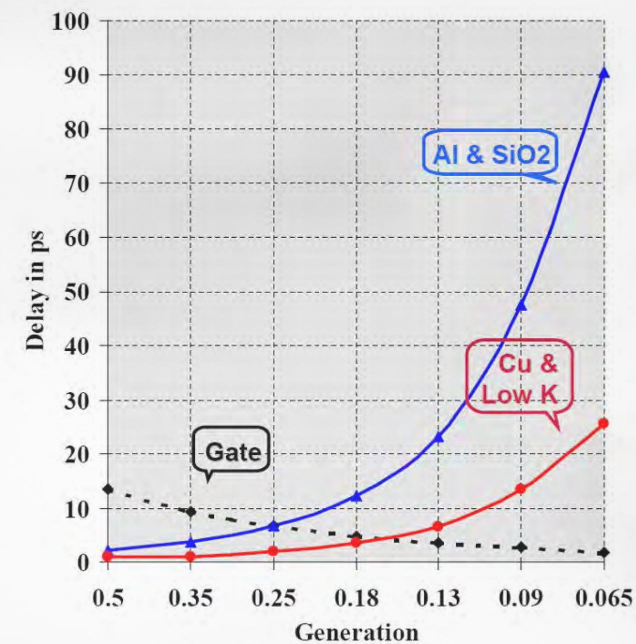
COMPETENCES

15 years ago, a remarkable step was taken by implementing copper as metallization material in the fabrication of integrated circuits (ICs). It was not only the change of material from aluminum to copper but rather the whole integration scheme, changing from the subtractive structuring method to the damascene process, that challenged engineers and scientists. However, especially the integration of new processes like CMP (chemical-mechanical planarization) and the development of new material combinations proved the superiority of copper against aluminum metallization.

In the early years of chip manufacturing, the transistor size determined the processor clock rate. A decreased gate length allowed a shorter switching time, which made the processors faster and faster. However, a side effect of shrinking gate lengths is that the area available for electrical contacting is reduced as well. The wires as well as the spaces between them get smaller and reach the dimension of actual copper grain sizes, leading to a non-linear resistivity increase as well as increased capacitance effects.That means, nowadays, the signal propagation rate through the electrical wires limits the processor clock rate, since it passed the transistor switching time delay (Figure 1). Thus, the main task for research and development in the back-end of line is to minimize the RC delay. This is addressed through all different processes in the back-end of line module at the Fraunhofer CNT.



2 *Dual damascene process flow in the back-end of line. 1: ULK and hardmask deposition, 2: lithography, etch and cleaning, 3: barrier and seed layer deposition, 4: copper plating and anneal, 5: copper and barrier CMP.*



1 *RC delay influence of front-end of line transistor and back-end of line interconnects. Effect of change to copper and low-k. From: Bohr; „Interconnect Scaling – The Real Limiter to High Performance ULSI"; Proceedings of the 1995, IEEE International Electron Devices Meeting.*

The capacitance C can be decreased by using low-k materials as dielectrics. Besides changing the material type, porosity can be introduced to further decrease the k-value. However, a porous material increases the integration complexity, because all connected processes need to be tuned as to minimize the damage of the porous material itself and the k-value degradation. Furthermore the mechanical strength of porous low-k material can be challenging.

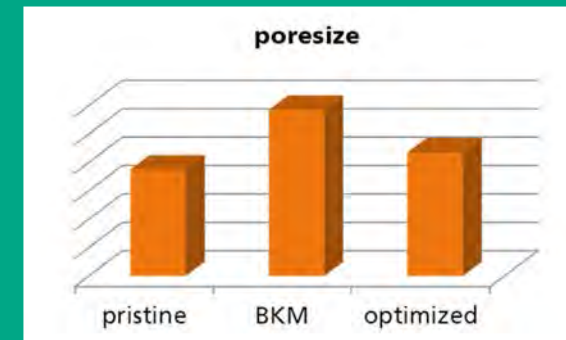
At the Fraunhofer CNT research focus has been put on the sidewall damage of the low-k due to the RIE etch, the influence of wet clean processes after dry etching and the possibilities of restoring k-values through repair processes. For the future it is intended to investigate the influence of CMP processes on the k-value.

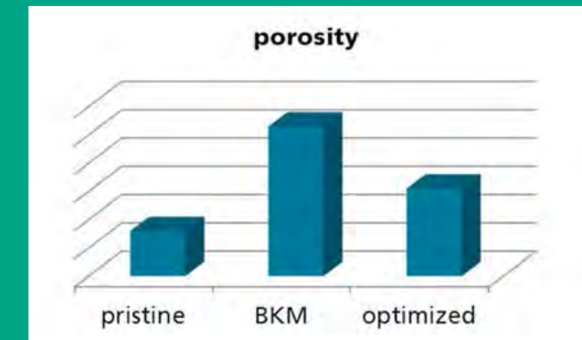
The resistivity R depends on the materials used for metallization and their microstructure. State-of-the-art material for leading edge interconnect technology remains copper. Its specific resistivity is low (1.7 µΩcm) and electro- and stress migration are sufficient. However, copper needs an efficient barrier to prevent it from diffusion into the interlayer dielectric and to prevent it from oxidation. It is the aim of interconnect integration to use as much copper for the circuit as possible for performance and as little barrier as absolutely needed for reliability. As the cross-section of connects for leading edge technology nodes is in the order of copper grain sizes and the barrier uses a significant area fraction, barrier material reduction and void-free copper filling with optimized microstructure is demanded.

Thus at the Fraunhofer CNT focus is on the development of new CVD-deposited barrier materials, that allow a thin and conformal deposition with good sidewall coverage. Preferably, these barriers have value added properties like good conductance to omit a seed layer for copper deposition, which, together with a void-free copper superfilling by electrochemical deposition, leads to a better copper microstructure and thus faster and more reliable circuits. The role of the bath additives in electrochemical plating, which are responsible for superfilling, is subject of research at the Fraunhofer CNT. Furthermore the influence of the annealing regime on the copper microstructure can be studied.

In the near future process development in the field of chemical-mechanical planarization in interconnect technology can be carried out. Topics of interest will cover polishing of new barrier materials with low damage stop on low-k dielectrics. The back-end of line process flow is shown in Figure 2. Leading edge research in the Fraunhofer CNT covers ULK etch, clean, barrier and seed deposition, copper plating and CMP.

FUNCTIONAL ELECTRONIC MATERIALS - BACK-END OF LINE





3 *Retention of ultra-low-K structural properties by optimized etch process.*

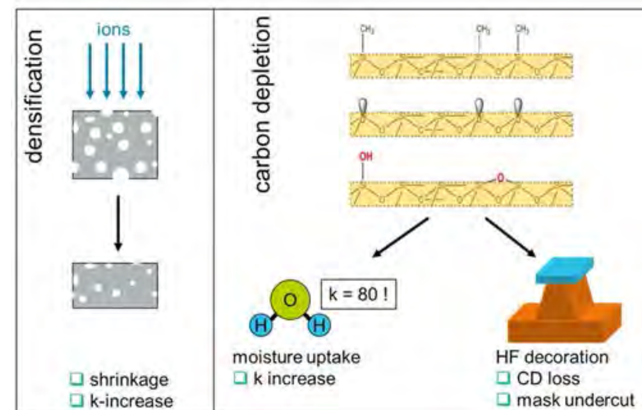
INTEGRATION OF ULK-PERFORMANCE

ULK Etch – Structuring of the Patterns

Vias and trenches in the dielectric are formed by reactive ion etching. The complex etching process proves to be especially challenging for low-k and ultra-low-k materials.
These new dielectrics introduce carbon to lower the polarizability and thus the k value down from 4 (traditionally used SiO_2) to about 2.7 for low-k materials. By adding pores, the so called ultra-low-k (ULK) materials achieve k values as low as 2. However, low-k materials come with several integration challenges, especially for the etching and resist ashing processes, which cause damages in the microstructure and alter the materials properties. Challenges are:

- Profile and CD control
- Change of dielectric properties by plasma induced damage leading to increased k value, which impacts the electrical performance
- Pore diffusion, moisture uptake, metal barrier precursor diffusion
- Sidewall and bottom surface roughness
- Mask integration
  - o Metallic hard masks: wiggling, μ-masking, metallic residues
  - o Organic resists: ashing, resist poisoning

Plasma damage can be divided into two mechanisms. The physical damage results from ion bombardment in the plasma. In low density porous low-k materials this leads to a densification and hence to a shrinkage and an increase in the k-value.
The chemical effect plays a more important role in the trench sidewalls. Here, the methyl groups of the ULK material (which are responsible for the lower k-value) can be removed by the



1 *Damage mechanisms during ultra-low-K etching.*

species in the plasma. This leads to dangling bonds or formation of hydroxyl groups at the surface. The result is a much more polar surface which leads to a much higher probability of water adsorption. With the adsorbed water (k-value of 80!) the effective k of the ULK material rises. Additional problems arise when the damaged ULK material is exposed to the subsequent cleaning step. Because damaged ULK is chemically similar to silicon dioxide, the cleaning step by hydrofluoric acid attacks the altered dielectric. This material removal can cause issues like hard mask undercuts or CD loss and further difficulties with the barrier layer deposition afterwards.

During an extensive project together with Globalfoundries details about the damaging of the ULK material by the etch process are investigated. Several advanced plasma diagnostics are available like high-resolution optical emission spectroscopy, quadrupole mass spectroscopy and quantum cascade laser absorption spectroscopy. Using these methods helps to understand the details of the processes, e.g. by detecting plasma species in the excited state and in the ground state.

Through our close cooperation with Globalfoundries and our equipment (300 mm industry standard) a complete back-end of line integration is possible. Processed wafers can be send back to Globalfoundries for further processing or for the measurement of electrical data, which provide the ultimate benchmark for refined or newly developed processes.

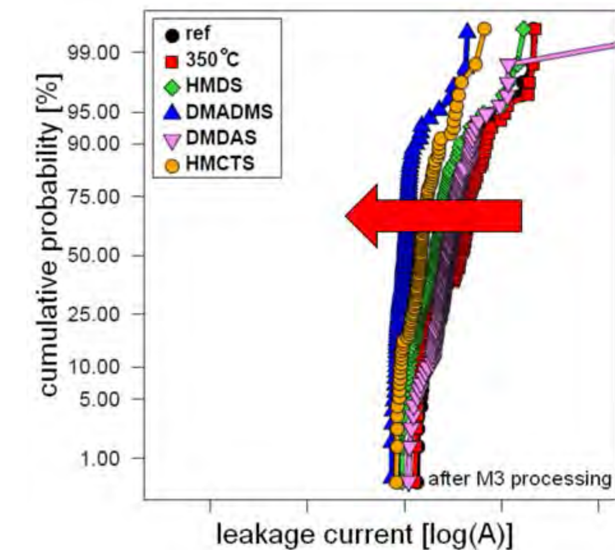
ULK Clean – Removing Etch Residues

After etching vias and trenches, the next step is usually a wet clean. Residues from hard masks, remaining resist or fluorine polymers formed on the sidewalls have to be removed to enable a clean and conformal deposition of the barriers afterwards.
Several different cleaning chemicals, water or solvent based are evaluated with special emphasize on compatibility with the ULK material, copper and the barrier layers. Since the structures get smaller and smaller, good surface wetability has to be assured. Adding surfactants and optimizing process parameters for chemistry application and rinsing steps can improve the overall performance of the ULK cleaning step.

ULK Repair – Restoring the k-value

Though the etch process can be optimized to result in minimal damage of the ULK material, it may not be possible to completely keep the pristine structure of the dielectric. The aforementioned carbon depletion and water adsorption can be faced by chemical sylilation repair processes. Here polar hydroxyl groups are substituted by methyl groups and the original ULK structure and thus the k-value can be restored.

Similar to the cleaning step different repair chemicals can be screened to find the optimal process parameters. Additional pre annealing to remove adsorbed water and post curing by UV as well as IR radiation to remove unbound fragments and to promote cross linking can be used.



2 *Improvement of leakage current by low-k repair.*

ULK Characterization – Observing material changes

Furthermore there are multiple options for advanced ULK analytics. A unique tool is ellipsometric porosimetry which enables pore size and porosity measurements. Additional information about the Young's modulus or diffusion barrier integrity can also be obtained. Via different TEM options like EELS or EDX the carbon loss in the ULK material which is associated with plasma damage can be measured. Finally by FTIR the character of the chemical bonds in the ULK material can be identified.

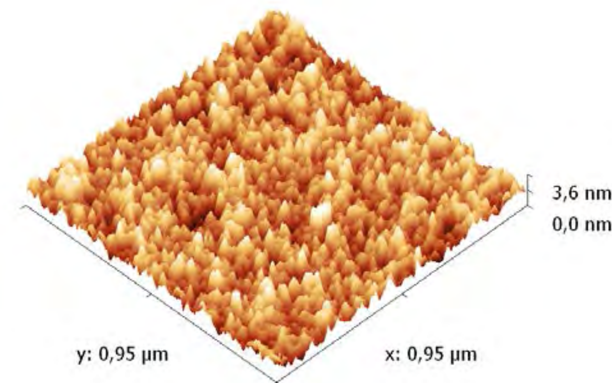
By optimizing existing 'best known methods' (BKMs) recipes an improvement for the etching of the ULK layers can be achieved. The optimized processes yield ULK films with a structure much more similar to the pristine one, in terms of pore size or porosity, while maintaining a comparable etch rate (Figure 3).

FUNCTIONAL ELECTRONIC MATERIALS - BACK-END OF LINE

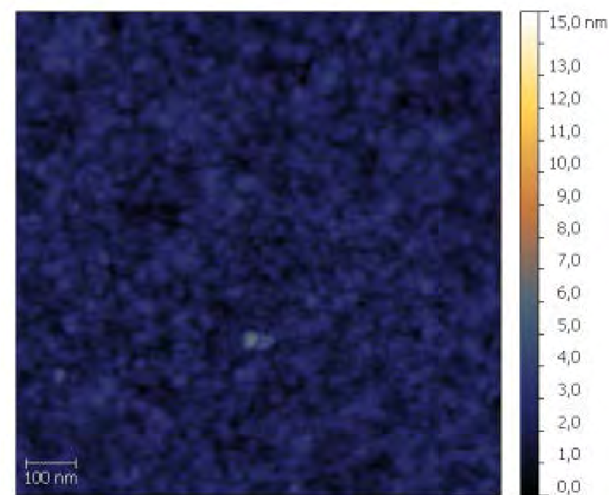
COPPER DIFFUSION BARRIERS SCALING

The transition to the Cu/ULK node induced a need for the development of novel diffusion barriers preventing the intermixing of copper with the adjacent dielectric layer and other regions on the chip. They should be compatible with current integrated circuit fabrication flows. At the same time the material used needs to be thermal and structural stable and also highly thermally and electrically conductive.

The present state-of-the-art barrier/adhesion promoter used in the back-end of line is a Ta/TaN film stack. However, despite its excellent barrier properties, this material combination has also some limitations. One of them is given by the fact that both, the Ta and TaN are deposited by physical vapor deposition (PVD). This deposition technique does not comply with the stringent step coverage requirements for features having critical dimensions. Furthermore, the copper plating can not be conducted direct on the Ta layer. First a seed layer has to be deposited. By this way the trench fraction that is filled with bulk copper is reduced and the resistivity of the whole interconnect structure increases.



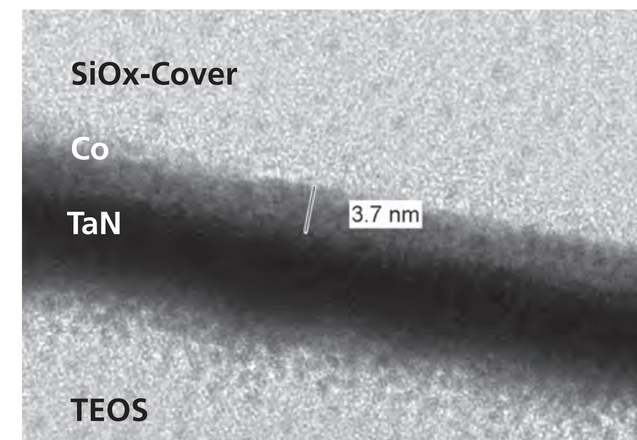
1 B *AFM measurement of a 7.5 nm thick cobalt layer*



1 A *AFM measurement of a 7.5 nm thick cobalt layer.*

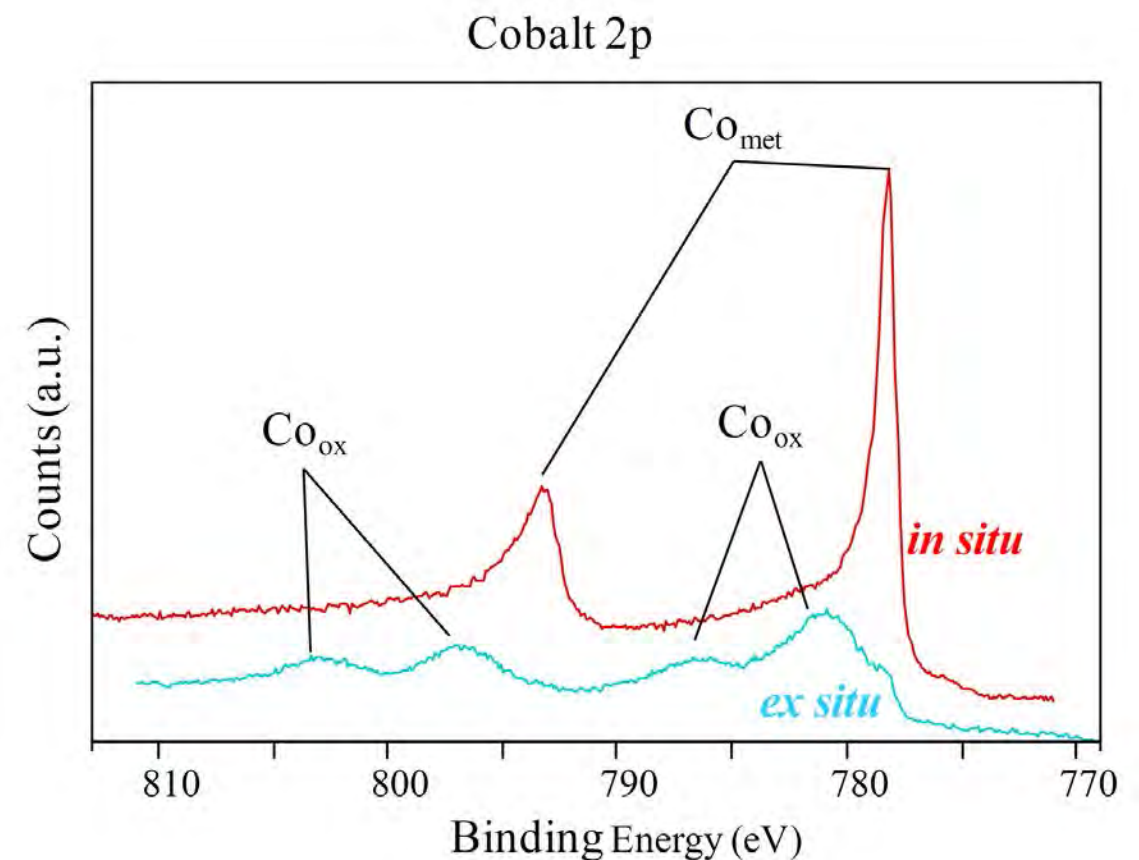
To overcome these limitations Fraunhofer CNT and GLOBAL-FOUNDRIES have joint their efforts to enable chemical vapor deposited (CVD) cobalt as the diffusion barrier of choice for sub 28 nm technology nodes, see Figures 1 and 2 for topography measurements by AFM and a TEM cross section, respectively. Compared to Ta it has a much lower electrical resistivity and higher thermal conductivity, but the greatest benefit of introducing Co as a barrier material is given by the fact, that it can be deposited by CVD and the Cu plating can be conducted directly on its surface.

In this way the step coverage of structures with critical dimensions can be improved and the trench fraction filled with bulk copper, thus the electrical conductivity of the conductor path can be increased.



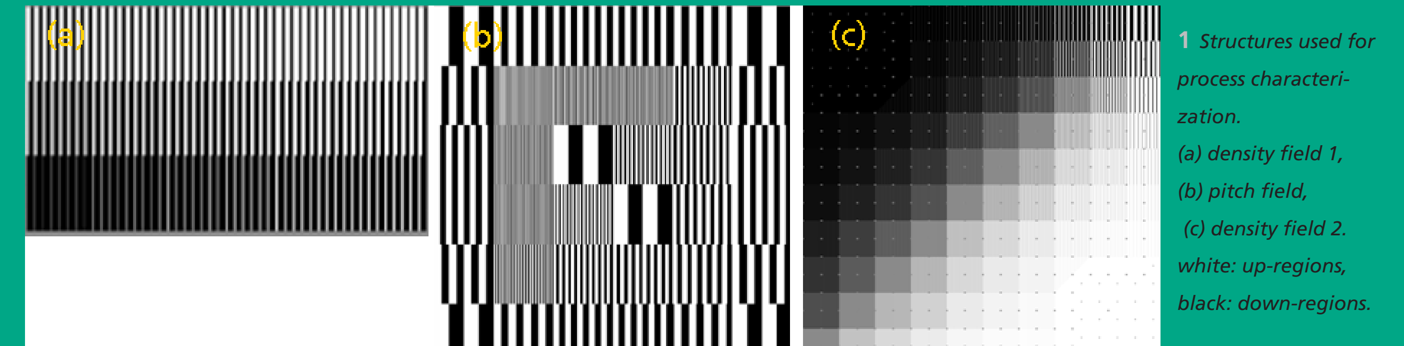
2 *TEM of a Co layer deposited on TaN.*

For process development and optimization Fraunhofer CNT uses a state-of-the-art AMAT Endura2 tool having Degas, PVD Ta/TaN, PVD Cu RFX and CVD Co chambers. One additional advantage is given by the in situ XPS measurement system enabling chemical analysis of the deposited thin film layers without breaking the process vacuum. The importance of in situ XPS is shown in Figure 3: exposure to air during ex situ measurements leads to a rapid oxidation of the Co surface.



3 *In situ and ex situ XPS measurement of a cobalt layer.*

FUNCTIONAL ELECTRONIC MATERIALS - BACK-END OF LINE



1 *Structures used for process characterization. (a) density field 1, (b) pitch field, (c) density field 2. white: up-regions, black: down-regions.*

FROM POLISHING TO HIGH PERFORMANCE PLANARIZATION

As the size of modern integrated circuits continues to shrink, the planarity of structures after CMP becomes more and more important. As a result, a better understanding of the relevant mechanisms affecting planarization is needed in order to meet future process specifications.

The planarization of a patterned wafer is characterized by the interaction of numerous variables such as applied pressure, relative velocity between pad and wafer, pad (roughness, hardness, elastic modulus, etc.) and slurry characteristics. In respect to pad surface roughness, a conditioning process is performed in order to remove debris from the pad surface, restore pad surface quality and thus to achieve high and stable removal rates from wafer to wafer.

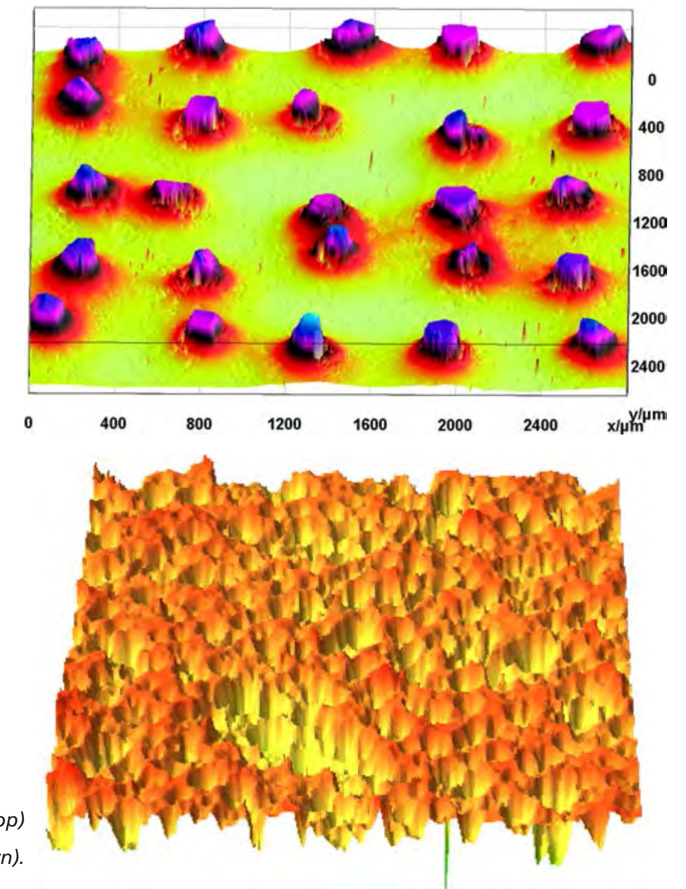
Thus, a small amount of pad material is continuously removed and the specific pad surface properties are established. Because only this modified upper pad layer, defined as 'asperity layer', contacts the wafer during polishing, it has a large impact on the quality of the CMP process. To characterize the interrelation between conditioning and pad surface texture, a novel roughness characterization methodology has been developed. It is capable of extracting important contact mechanical parameters like the mean asperities radius of curvature, the asperity height and size distribution. These pad properties can be linked directly to process characteristics like removal rate, defect density and planarization performance in CMP and thus be used for consumables testing and optimization (Fig. 3).

Another topic in which the Fraunhofer CNT has large experience is the characterization of the CMP planarization performance. For this, the influence of consumables like slurry, pad or conditioner on the planarization of specifically developed CMP test-wafers is systematically examined and evaluated using in house developed analysis routines.

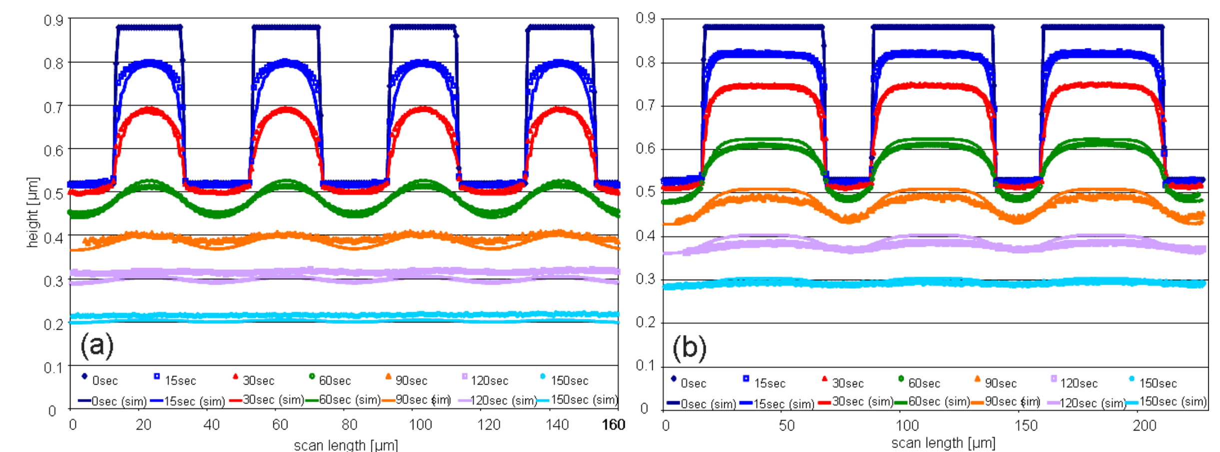
Stringent requirements of newest technology nodes as well as the transformation of traditional IC manufacturing towards foundry businesses with a wide and rapidly changing product portfolio, in extreme cases with little quantities, the ever decreasing time to market and shortened product life time of chip generations, all these demand a well-aligned CMP design and process. Thus a CMP-aware design becomes more and more crucial to be capable of competing on the market.

Novel CMP modeling approaches are a powerful tool for achieving this goal by enhanced process understanding, therefore enabling new integration paths, precise design rules with fill strategies and cost effecient process development. The Fraunhofer CNT has great knowledge in the characterization of planarization processes with the help of patterned CMP test chips (Fig. 1). The data collected is used to build up chip and feature scale CMP models, which are capable of simulating the characterized planarization process. Such calibrated models can be used on real production layouts to identify hot spots and support smart fill strategies or suggest design changes before the production of the mask sets.

2 *CMP equipment at the Fraunhofer CNT: (left) Applied Materials Reflexion LK; (right) Stangl mobile slurry systems.*

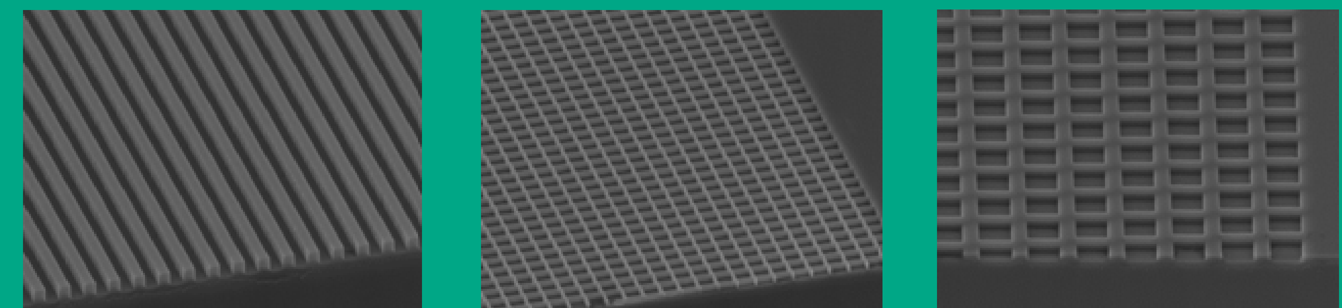


3 *Confocal measurements of a conditioner (top) and a 1 mmx1 mm conditioned pad sample (down).*



4 *(left) Measured (symbols) and modeled planarization of test structures with 20 µm line width, 20 µm space width and 50 % density. (right) Measured (symbols) and modeled planarization of test structures with 50 µm line width, 20 µm space width and 71.4 % density.*

COMPETENCE AREA MASKLESS LITHOGRAPHY



2 *Imprint template structures transferred into silicon*

Group Manager
Patterning

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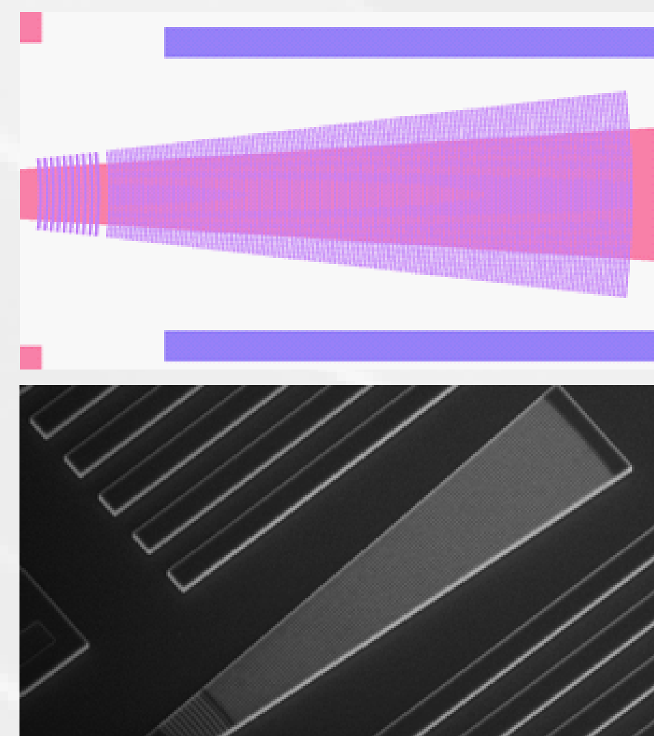
COMPETENCES

The competence area "Maskless Lithography" provides manufacturing of resist masks in special organic photoresists with patterning sizes down to 35 nm and their transfer into the underlying hard mask. Exposure is carried out using maskless electron beam lithography. The competence area focuses on the preparation of customer and application-specific designs and layouts on 200 mm and 300 mm wafers via a modern and flexible direct patterning process.

TRENDS

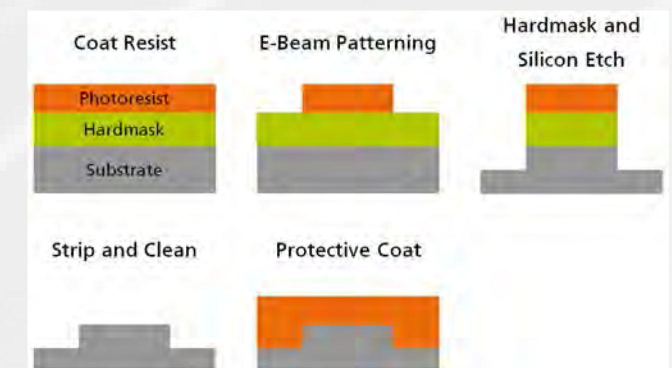
In 2011, Fraunhofer CNT's patterning capabilities have been extended to meet customer requirements according to high resolution "More-Moore" applications but also for novel "More-than-Moore" challenges. Research in the field of e-beam patterning has been intensified regarding resist resolution, data prep and proximity effect correction (PEC) as well as most advanced e-beam lithography processes on customer specific substrates and stacks.



3 *Optical coupling as designed (left) and as final imprint template (down)*

MANUFACTURING OF NANOIMPRINT TEMPLATES

In 2011, Fraunhofer Center Nanoelectronic Technologies (CNT) started activities in the field of production of nano imprint master templates in close collaboration with various customers. The main task was to implement a suitable process for short reaction times to layout changes and fast production of the resist masks for further processing. First experiments with a simple hardmask and resist stack as shown in Figure 1 yielded promising results for a wide range of features such as line space structures and large lattice or pillar arrays.
This process takes advantage of existing knowhow at Fraunhofer CNT, especially the flexibility of the Vistec SB3050DW shaped electron beam lithography tool which allows almost any feature to be written directly into the resist on the same wafer. After the lithographic patterning, the structures are transferred into the silicon by a hardmask etch process.
This allows precise depth tuning for the imprint template with very good depth uniformity and steep sidewall angles. This in turn ensures a high structure quality over the entire template area. Example SEMs of finished template structures are shown in Figure 2. Because of the silicon structuring, the produced templates are very durable. After finishing the structuring of the templates, an additional organic layer is spun on top of the product in order to protect the surface from damage or particles. In this state they can also be cleaved to the required size in order to be ready for usage at the customer's site, where the protective coat can be easily removed with standard solvents. This post-structuring handling process is designed to ensure very low defectivity on the delivered templates.
The production of multilayer imprint masters takes the template production one step further. A multilayer template eliminates the issue of overlay while producing with two separate templates at the cost of a more complex production cycle of the template. We successfully integrated a two-layer-template with our partners Fraunhofer Institute for Photonic Microsystems (IPMS) and the Technical University Dresden.



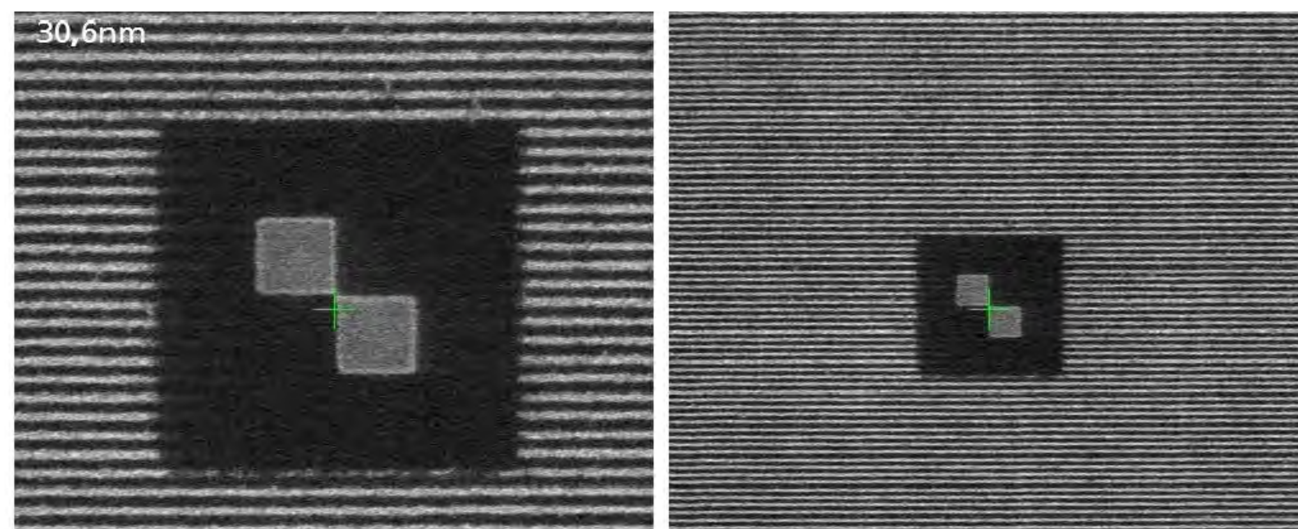
1 *Schematic process flow of imprint production*

The first step structured a waveguide into the silicon, shown as pink bars in Figure 3. The second layer (purple) structured a coupling on top of the waveguide in order to allow signals of a certain wavelength to be coupled into the substrate. Waveguides and couplings were printed in a wide range of sizes to allow fine tuning of wavelengths and to be able to characterize the waveguide behavior. An example of the produced patterns is shown in Figure 3 *(left page)*.
It shows the layout of the coupling on the left and the produced imprint template on the right. This feature contains a curved shape which was easily patterned via a gds layout provided by our partners, who had free hand in designing their template. In case of layout problems, adjustments and changes can be implemented onsite within minutes to ensure that only correct patterns are printed.
The constantly monitored processes at Fraunhofer CNT enable a quick and precise integration of both layers on the silicon substrate. Direct write lithography at Fraunhofer CNT is currently possible on 200mm and 300mm wafers on a production-like flow. In addition.wafer sizes down to 100mm can be handled for rapid prototyping applications enabling cost-effective and flexible direct writing for many R&D scenarios.

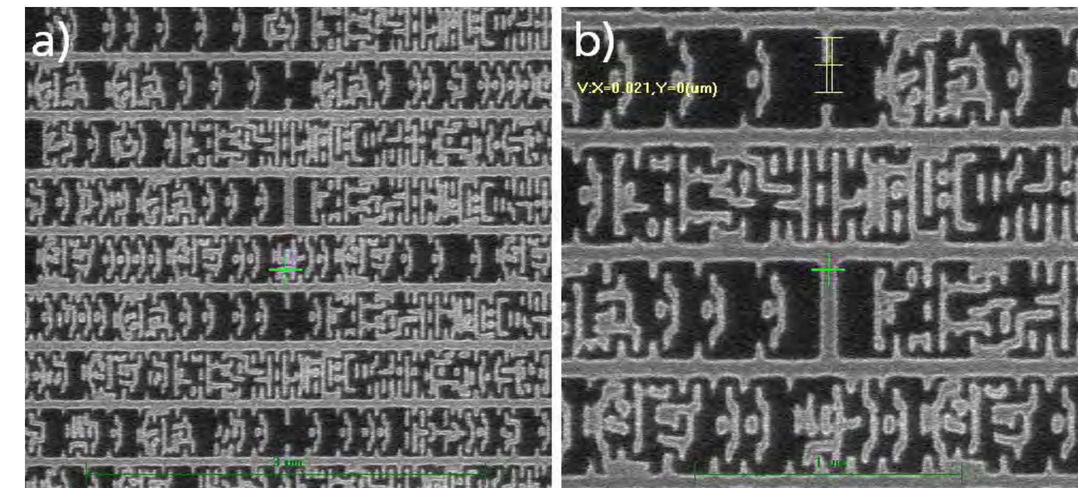
EVALUATION OF DIRECT PATTERNABLE INORGANIC SPIN-ON HARD MASK MATERIALS USING ELECTRON BEAM LITHOGRAPHY

Resist patterning on wafers using e-beam lithography is an alternative to optical lithography. Especially for rapid prototyping applications with very small wafer volume, electron beam direct write (EBDW) has certain advantages. For example, design changes can be implemented overnight and verified before mask tape out, different design versions can be tested on one wafer or design bugs can be corrected (especially metal fix). EBDW provides high resolution and the variable shaped beam systems have higher throughput compared to Gaussian beam systems. Furthermore, mask costs are saved and mask delivery delay is removed.

For the 22nm node, the ITRS roadmap includes mask less lithography (ML2) using multi beam technologies. High resolution e-beam resists are needed for ML2 to reach the requirements of the ITRS. Chemically amplified electron beam resists are fulfilling sensitivity requirements for e-beam direct writing but are limited in resolution due to acid diffusion. Stowers et al have shown electron beam exposure results using inorganic non-chemically amplified resists based on hafnium and zirconium oxides with high resolution and higher sensitivity compared to state of art non-chemically amplified resists like hydrogen silsesquioxane (HSQ).
Fraunhofer CNT investigated a new inorganic non-chemically amplified resists provided by Inpria Corp. and compared them with two other high resolution resists: HSQ and a negative tone chemically amplified resist (nCAR). As a metal oxide, the resist has high etch resistance comparable to hard mask materials and is a promising candidate for e-beam lithography as well as for EUV lithography. With the variable shaped beam at Fraunhofer CNT 1:1 dense pattern with a dimension of 100 µm x 100µm were exposed. In Figure 1 exposure results



1 *XE15IB SEM images of 1:1 dense pattern with feature CD 30nm (measured CD mentioned top left)*



2 *XE15IB SEM images of 22nm SRAM pattern (FOV 4µm (a) and 2µm (b)), layout courtesy of GLOBALFOUNDRIES*

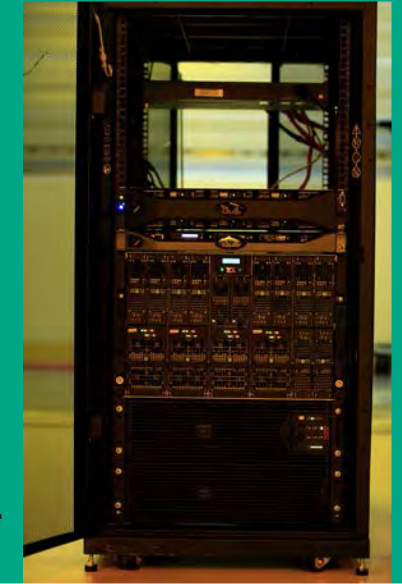
of that 1:1 dense pattern for 3 different feature CDs are summarized. The patterns are almost on target. A proximity effect correction for 1:1 dense pattern is not needed. XE15IB is able to resolve easily 30 nm of these large dense patterns. VISTECs SB3050DW was designed for the requirements of the 50nm node and reaches its tool limitation exposing 30 nm pattern and below. A resolution of 30nm hp dense lines was never achieved before with this tool at Fraunhofer CNT.

The slight stitching visible in the pictures comes from the electron beam and can be minimized. For comparison HSQ is able to resolve 35nm only (55nm film thickness and concentrated development with 25% TMAH) having no resolution to obtain 30nm. K. Steidel has shown in her Ph.D. thesis that the nCAR has a minimum resolution of 40nm for 1:1 dense lines. A large real application pattern is also demonstrated. The chosen pattern is a real SRAM metal 1 layer for the 32nm technology node. This layer was shrinked down to 22 nm feature size.
The pattern was proximity effect corrected with general proximity effect correction (PEC) parameters for non-chemically amplified resists. The design and SEM images of the SRAM pattern are shown in Figure 2. While the feature CD is on target, it is clearly visible that some lines are not correctly resolved or spaces are merged. Correct PEC parameters can improve the resolution and will be determined for the Inpria resist in the next steps. Fraunhofer CNT evaluated XE15IB in a near production environment. The resist is based on hafnium oxide as a direct patternable spin on hard mask. To investigate resolution and delay stabilities such as vacuum delay and shelf life, Contrast pattern, 1:1 dense lines and a SRAM metal 1 layer were exposed.
The contrast of XE15IB is about 50% better than HSQ and the dose is comparable. XE15IB shows good resolution for 22nm SRAM pattern. Compared to HSQ and the nCAR, XE15-IB has a better resolution for large 1:1 dense pattern. 30nm half pitch lines are resolvable. Shelf life and vacuum stability of XE15IB does not yet meet the requirements for a shelf life of several months and a vacuum delay up to one day. By improving the resist process or by sizing the dense structures the pattern quality of the 30nm lines is expected to become improved down to 27nm.

A further resolution improvement of the SRAM features can be obtained by applying the correct proximity effect parameter. A significant advantage of a hafnium oxide based resist compared to others is the etch selectivity so that relaxing the film thickness is prevented from pattern collapse. In future research activities etch performance (selectivity to Silicon) has to be proven and additionally LWR and LER have to be investigated at Fraunhofer CNT.

MASKLESS LITHOGRAPHY

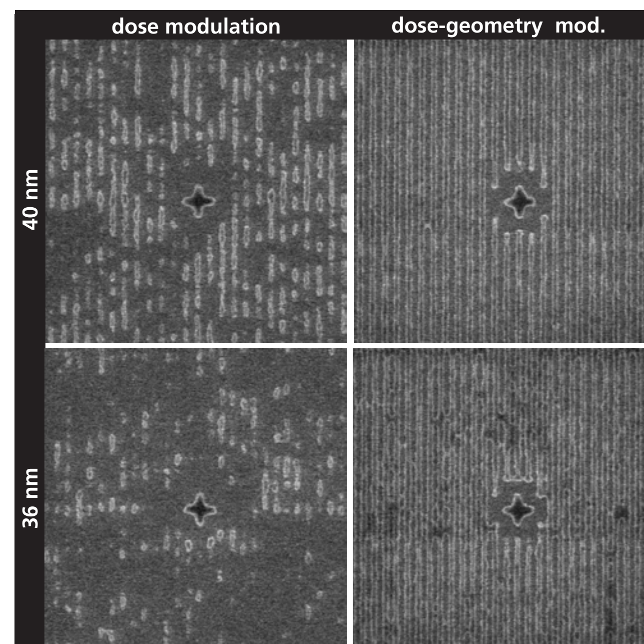
Novel 64bit-high performance cluster device for e-beam data prep



UPGRADE OF THE DATA PREPARATION ENVIRONMENT FOR CNT'S E-BEAM LITHOGRAPHY

The data preparation for e-beam lithography is an essential technological component and needs to be improved similarly to improvements of resist resolution or the resolution of the exposure tool. To fulfill the requirements and demands of upcoming semiconductor technology nodes and other customers of e-beam lithography, Fraunhofer CNT upgraded its former 32-bit data preparation cluster environment in 2011. The new high performance cluster, which was set up for new data preparation software, is equipped with a master node and four computing nodes with Graphics Processing Units (GPUs) based on a 64bit Linux operating system. The accessible memory and computing power enables the processing of huge amounts of data which are common in semiconductor industry and increase with upcoming technology node. The investment for the DataPrep hardware was funded by BMBF/SMWK within the BRIDGE project.

The data preparation software, which prepares the exposure data using particular algorithms of proximity effect correction and fracturing, impacts the resolution, the exposure quality and its process window in e-beam lithography. Fraunhofer CNT is collaborating with ASELTA Nanographics, Grenoble, France for providing the creative solution for future sub-30nm mask writing and ML2 applications [Ref. Press Release]. This industrial cooperation not only aims at the development of proximity effect corrections but also tries to improve various practical factors in e-beam lithography, such as the shortening of writing time, speeding up the data preparation process, customization etc.
Through the co-work of Fraunhofer CNT and ASELTA Nanographics it was already proven that the exposure quality

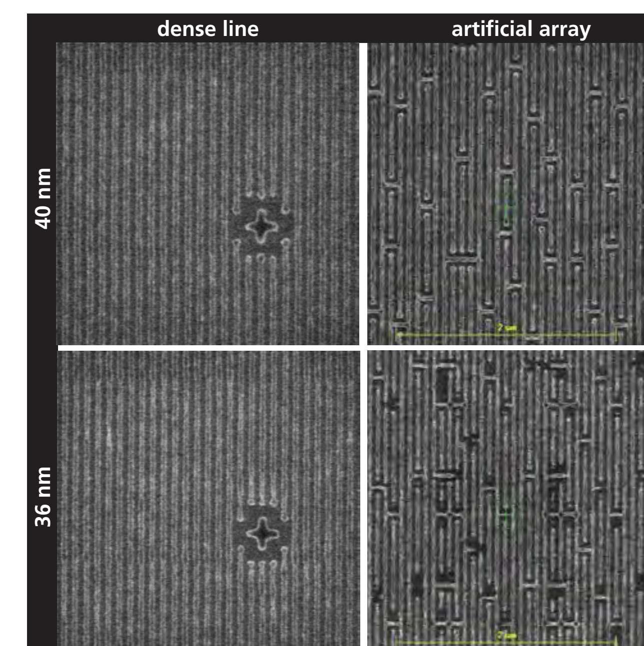


1 *Comparison of the simulations and test exposed images between dose modulated correction and dose-geometry modulated correction*

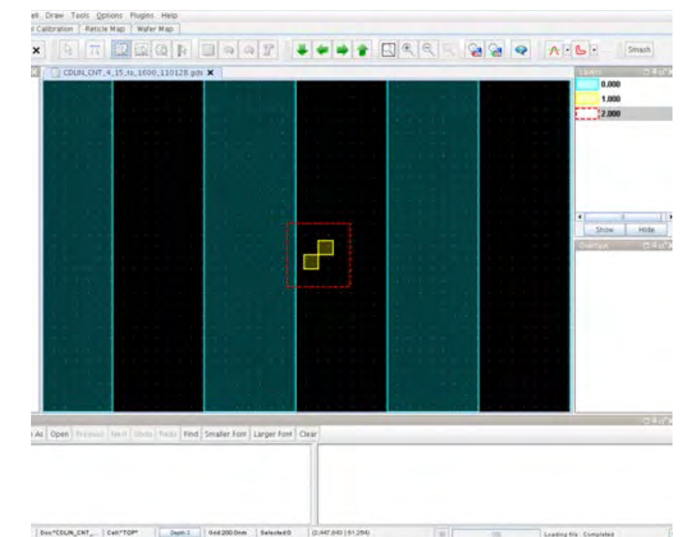
and capability in e-beam lithography can be enhanced by the newly developed data prep software INSCALE®. [Ref. Proc. SPIE Vol.8166, 816621, 2011.] Furthermore it either can amend the real application factors of e-beam lithography, like calculation time, the influence for writing time etc. The collaboration between Fraunhofer CNT and ASELTA Nanographics is ongoing to refine the innovative data prep solution and to make it fit for next technological nodes and ML2 applications. Aselta Nanographics developed the new type of algorithm called electron Resolution Improvement Features (eRIF), which bases on the dose modulation and multiple pass exposure.

Figure 2 presents the test pattern images, exposed and observed at Fraunhofer CNT and corrected with eRIF. With the application of eRIF, test patterns are clearly resolved not only on the dense lines of 40 nm but also on that of down to 36 nm. The artificial arrays of 40 nm test patterns are also resolved with good qualities.

The test artificial array with the design CDs of 36 nm are observed as enhanced its quality of exposures but with some glitches. It is considered that these are not just due to the capabilities of data prep but also the susceptibility of process in the applied nCAR is getting to reach its boundary. Though the observation of test exposure that is obtained in the artificial array of 36 nm does not seem perfect, the eRIF is able to demonstrate that the data prep can make the exposures possible for a technology node beyond using current exposure tool and its processes.



2 *SEM images of test exposed patterns corrected and prepared with eRIF and Inscale®.*



3 *Screenshot: graphical user interface (GUI) Inscale Software*

One of the promising candidates for the real application in e-beam lithography in near future is complementary exposure, especially for the high volume manufacturing in future technological node. Because of the characteristics of its application, the design consists not simply of the line repetition but of the complicated combination of lines, polygons, elongated holes and holes. To achieve the usable corrections for those, the various correction redundancies, which means not only of CDs but also for corner rounding and LES, are required.

This means the correction algorithm itself should be more weighted to 2-dimensions than the 1-dimensional way. It is the reason why eRIF is considered as beneficial to this application. Figure 2 exhibits the images of exposed test patterns, which are corrected by eRIF, along with the simulated resist contours after the correction. Those are further enhanced than the images obtained from the patterns that are corrected using dose-geometry modulations, which are not shown in here, when they are cross-examined in comparison.

COMPETENCE AREA DEVICES & INTEGRATION

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COMPETENCES

The main research topic of the competence group "Device & Integration" is the development and integration of nanoelectronic process modules and devices. There, the focus is on the electrical characterization of semiconductor devices on wafer level such as memory devices (single memory transistors, arrays and demonstrators) as well as on the development of concepts for the integration of new materials and innovative etching processes in process flows in order to fabricate nanoscaled structures. The design and fabrication of test structures and test chips enables fast learning cycles for process development.

TRENDS

With the recent developments in integrating new thin-film materials such as high-k gate dielectrics, many process integration issues have to be solved in order to meet the reliability targets and to benefit from a low power consumption and high-operating frequency of devices in the 2x nm scale. For structuring the new materials, advanced etching processes needs to be developed for achieving good uniformity and low damage of adjacent structures. The etching plays also a big role in the fabrication of deep trenches with small diameter that are used for 3D-capacitors but also for the TSV packaging technology. Here, research is focusing on gaining high aspect ratios while maintaining smooth trench surfaces.

The electrical characterization is addressing the challenges of the new materials and processes. Therefore, advanced reliability characterization methods of high-k materials and the development of new test structures for process monitoring are on the roadmap as well as the investigation of reliable probing and testing on small contact pads that are important to reduce the chip-area and to enable new packaging

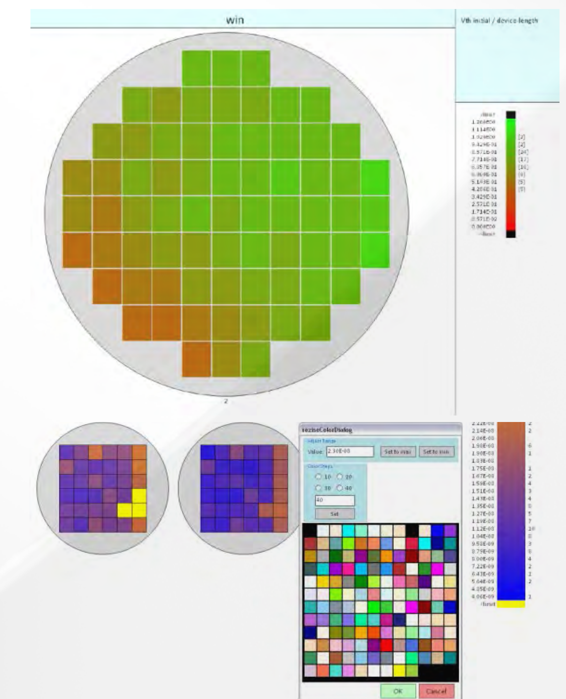
FLEXIBLE WAFERMAP SOFTWARE

Due to the lack of suitable free and commercial software tools to analyze and visualize test data as a wafermap, the CNT D&I group designed and programmed a software tool that can collect and visualize measured physical or electrical parameters on device level. The aim of such software is to map measured data of semiconductor structures to the physical positions on the wafer. This kind of visualization helps to find trends or outliers of physical or electrical parameters across the wafer and hence to find possible problems in the production process. The primary goal was to design a tool that can handle measured data of discrete semiconductor devices and test structures (regularly spaced date without interpolation in between), e.g. CMOS transistors, memory devices like FeFET, standard Flash and TANOS flash cells as well as capacitor structures like "MIM" or "MIS".
To be able to handle different kinds of data from different types of test equipment the tool needs a flexible interface for the data import. Furthermore it needs to be flexible and extendable enough to support future test data formats.

Other requirements are:

- Easy user interface that supports a fast and straightforward workflow
- Automatization capability: Perform repeating wafer mapping operations automatically that requires only a small amount of effort from the user
- Different types of output formats (reports)

The CNT wafermap software supports two types of operation modes: Interactive mode and scripting mode. In the interactive mode the user manually adjust the data import and the visual appearance of the result with a GUI designed for that purpose. This is the fastest way to produce a result in only a few minutes. The user can adjust the color mapping and a few of the most important parameters for the visual style. This mode is like a fast preview mode due to its limited number of adjustable parameters. The second, much more powerful mode is



1 *A typical wafermap generated by CNT Wafermap (up), CNT Wafermap interactive mode (down)*

the scripting mode. The CNT wafermap tool can be controlled by a specially designed scripting language (batch-style). The integrated script editor allows to load, save, edit and run such scripts. With more than 20 keywords the user can control all parameters for data import, export and the visual appearance of the wafer map.
Additionally, the script mode is partly interactive by allowing the user to click on certain keywords which opens a suitable window to make adjustments to the keyword parameters (e.g. clicking on a color statement would open a color picker). The output generated by the script can be previewed before being exported to an external report file and the user can browse through the generated wafermap sheets. Thus, the user has a fast feedback of the result in a comfortable and easy to use development environment.

DEVICES & INTEGRATION

ADVANCED MEMORY DEVELOPMENT

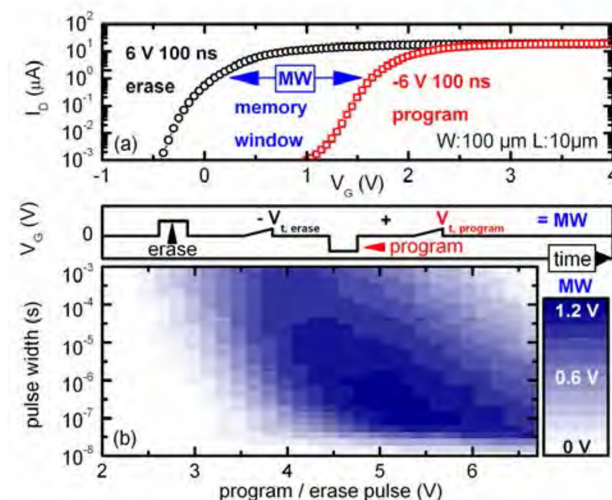
Since conventional memory technologies such as floating gate flash are facing severe problems below technology nodes of around 3xnm and beyond, manufacturers of nonvolatile memories (NVM) are developing memory concepts which allow for further increase of cell density. These new concepts are often referred to as emerging memories. Also FhG CNT is involved in several projects investigating and preparing next generation NVM.

FeFET

One promising candidate for future nonvolatile memory is the Ferroelectric Field Effect Transistor (FeFET) which has been developed and manufactured in cooperation with GLOBALFOUNDRIES and NAMLAB gGmbH. At FhG CNT critical processes for the device performance were carried out such as deposition of the ferroelectric material and etch. Using various test structures and single transistors on the processed wafers FhG CNT conducted a part of the electrical characterization and optimization of performance parameters.

There, it was possible to verify the basic device operation which is representatively depicted in Figure 1a . Endurance comparable to current Flash technologies as well as data retention exceeding 10 years was further demonstrated. Additionally, outstanding switching times below 20 ns were achieved as can be seen in the time and field dependent memory window matrix in Figure 1b.

Using leading edge wafer test equipment all characterizations were also done on high statistics to ensure a balanced overview of electrical parameters.



1 *(a) Basic device operation of a ferroelectric field effect transistor (top). (b) Time and field dependence of ferroelectric switching and its impact on memory window evolution.(down)*

In summary this predicts a fast, highly scaled, non-volatile memory concept based on a highly engineered, ferroelectric HfO2. In current and future projects a 100 bit demonstrator will be fabricated representing the final step in putting the newly discovered ferroelectric properties of HfO2 to a useful application in industrial scale.

Enery efficient non-volatile SRAM

FhG CNT is involved in the development of non-volatile SRAM (nvSRAM) at ANVO-SYSTEMS DRESDEN. The basic electrical characterization as well as reliability measurements such as program-erase endurance and data retention was conducted using automatic wafer testers in the CNT laboratory.

For this purpose a set of specific test programs was designed implementing the individual needs of this new memory technology..This non-volatile SRAM combines two proven technologies (CMOS-SRAM and SONOS non-volatile memory) into a new technology for fast, reliable and energy efficient memories.

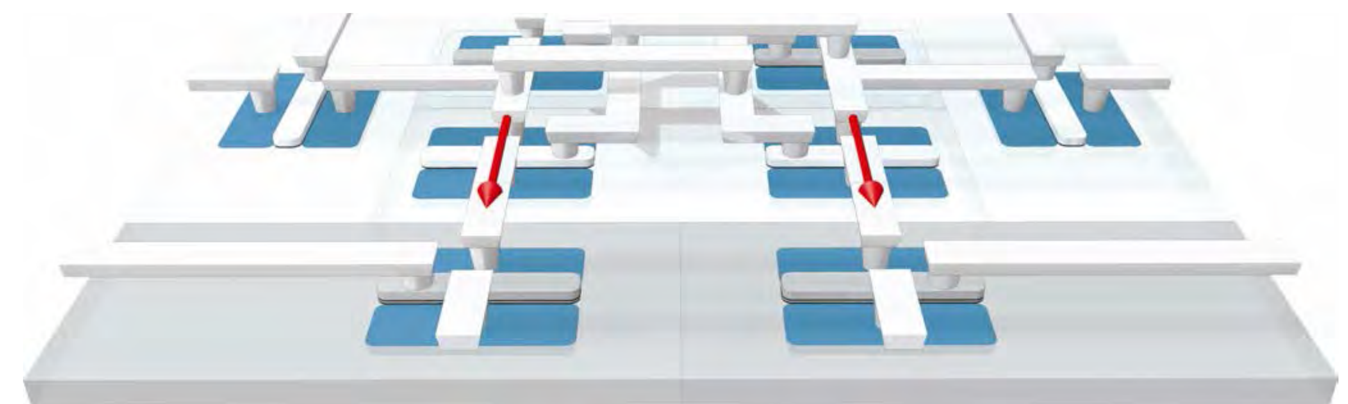
Due to unrestricted internal SRAM functionality, both fast reads and writes can be executed with the same high speed. The built in data protection is realized in a highly parallel internal architecture. An extremely energy efficient STORE mechanism enables the device to transfer the whole SRAM data to/from the non-volatile array in just one single step operation (8ms STORE / 10µs RECALL).

The obtained electrical data reveals a superior reliability of 20+ years data retention and practically unlimited write/erase endurance. Combined with extremely low power consumption at fast write speeds this nvSRAM addresses a wide range of applications.
It is ideally suited for self-powered and low power mobile systems in medical and automotive solutions but also as high speed non-volatile storage in industrial or computing applications.range of applications. It is ideally suited for energy autarkic and low power mobile systems in medical and automotive solutions but also as high speed non-volatile storage in industrial or computing applications.

3D NAND Flash Memory

Another aspect of manufacturing nonvolatile memories is the scalability of the device. Due to technological limits and emerging costs for planar memory arrays there are various approaches to build 3-dimensional memory architectures. These new architectures are based on a vertical multi gate NAND-structure to increase the device density per chip by stacking memory cells.
The challenge in building such memory devices is here shifted from lithography to the etching process, which has to structure a multilayer stack consisting of SiO2 and amorphous silicon in the case of a BiCS (Bit-cost scalable) flash memory.

Within the GOSSAMER Project Fraunhofer CNT has focused in 2011 on selected topics related to the integration of 3D-structures in the BiCs flash memory concept such as multi stack etch, dielectric deposition and poly-Si vertical channel formation in memory holes. The test vehicle is based on a SiO2/Si multi-layer stack that mimics the horizontal control gate plates of memory cells separated by SiO2 insulator layers (Figure 3).



2 *Schematic of an nvSRAM cell (6 SRAM transistors and 2 SONOS non-volatile transistors)*

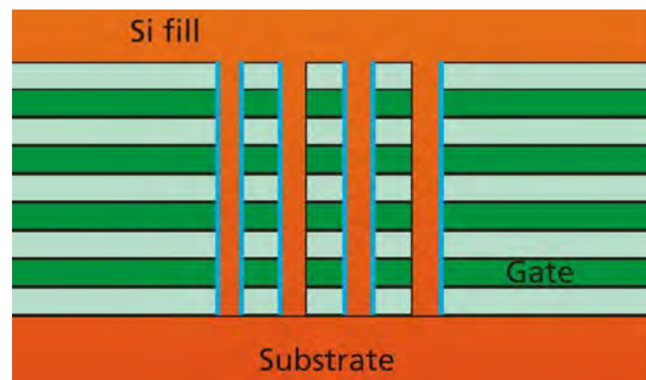
DEVICES & INTEGRATION

The major challenge in 3D NAND fabrication using the BICS approach is the high aspect ratio for dry etching of memory hole arrays into the a-Si / SiO_2 multi gate stack. Based on previously developed SiO_2 and Si single layer etch processes, a one-step etch process has been chosen as front up approach for the multi-stack open process.

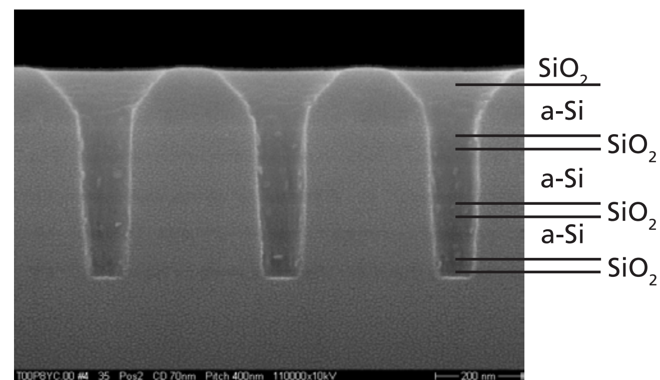
In this approach both materials a-Si and SiO_2 are etched within one process step. Advantages of this setup compared to multi step or multi chamber approaches are less complexity, higher manufacturability and low risk of defect density.

Two major topics have been identified as main challenges which are isotropic etch into the a-Si layer and etch selectivity to top hard mask. In order to decrease these effects several gas additives have been tested to sustain the passivation on the vertical silicon surfaces on the one hand and decrease the hard mask etch rate on the other hand. The optimized etch process shows promising results with sufficient selectivity and no silicon notching (Figure 4).

Additionally, processes for SiO_2/SiN/SiO_2 charge trapping stack fabrication were developed using the atomic layer deposition techniques to cover the sidewalls of the high aspect ratio device string templates. For Si channel formation a-Si deposition techniques were investigated including the selective epitaxy of Si to grow the Si channel vertically from the channel bottom.



3 *Schematic of test vehicle for 3D NAND flash development*



4 *Multi gate stack etch after optimization of the isotropic a-Si etch attack and selectivity to the SiO_2 hard mask.*

SHORT-LOOPS FOR ELECTRICAL MATERIAL CHARACTERIZATION

High performance and reliability as well as low power consumption are main requirements on the evolution roadmap of integrated circuits adding more functionality and processing speed to nextchip generations. In order to meet these requirements, material and interface properties of internal devices as in the gate stack of transistors or in integrated capacitors used in DRAM memories or in analog circuits - need to be optimized in each technology generation in parallel to downscaling of feature sizes. .

At Fraunhofer CNT processes for thin layer deposition of new and also conventional materials are evaluated and optimized for 300mm wafer fabrication and below for different chip applications.Besides uniformity or interface roughness, the electrical performance of conductance and capacitance as well as interface trap density or breakdown characteristics are key parameters studying the feasibility of new materials or processing techniques. In order to achieve fast feedback loops for customers' process and materials optimization different short-loop concepts are available at Fraunhofer CNT:

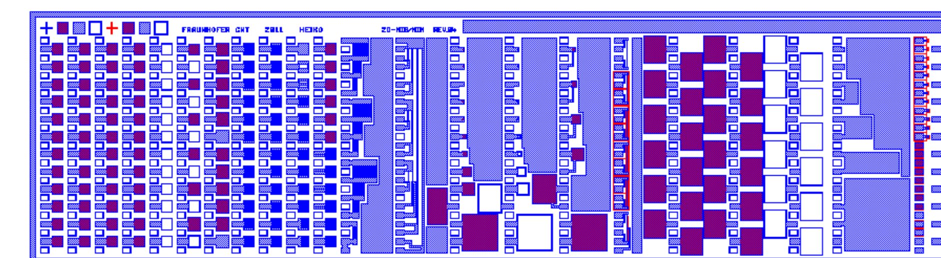
- Integrated planar MIS/MIM short-loop
- Metal dot deposition on MIS/MIM stacks
- MIS/MIM trench capacitor short-loop

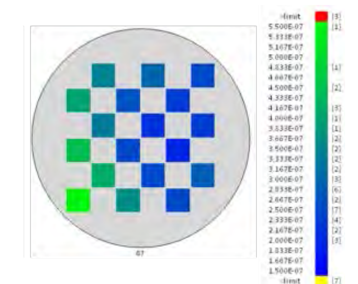
All three concepts are suitable for MIS and MIM stacks of various material compositions and will be described in the next sections.

Integrated planar MIS/MIM short-loop

This concept is based on a flexible test order This concept is based on a flexible test chip (Figure 1) comprising two lithography layers that are written maskless by e-beam lithography on many spots over the wafer, thus providing high accuracy and statistics for electrical characterization and delivering also information about uniformity characteristics of thin film layers over the wafer. The planar MIS/MIM testwafer are fabricated using 300mm wafer processing tools.

As shown in Figure 2 the MIS/MIM areas are surrounded by SiO_2 in order to achieve sufficient isolation between bottom and top electrode and to allow save contact by probe needles. Due to a standard contact interface the integrated MIS/MIM wafers can be measured on a fully automated probe-station using a probecard with 25 needles. This allows statistical reli-





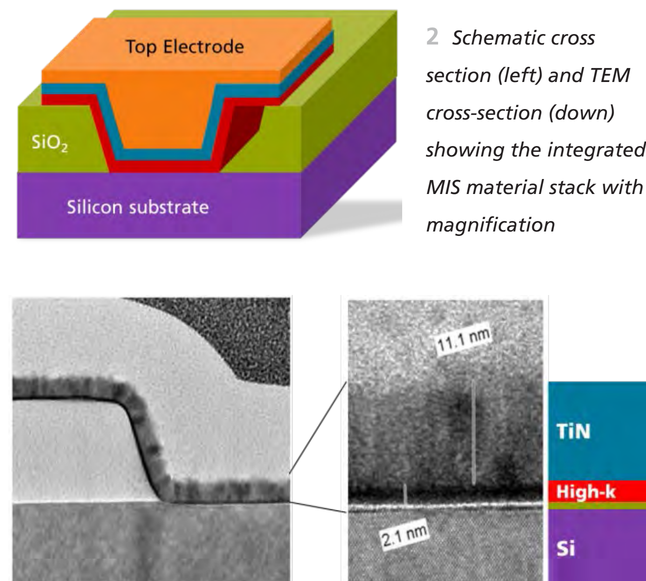
1 *Testchip Layout*

ability testing and material characterization in a temperature range from -55 °C up to 200 °C. Electrical measurement results of a MIS structure with high-k material as dielectric are shown in Figure 3. In the CV characteristic performance gain of high-k materials can be derived when transforming the measured capacitance into a theoretical equivalent thickness of SiO_2. That means, while maintaining same gate capacitance the high-k material can be much thicker compared to SiO_2 thus reducing gate leakage.current and finally power consumption of the devices.

Metal dot deposition on MIS/MIM stacks

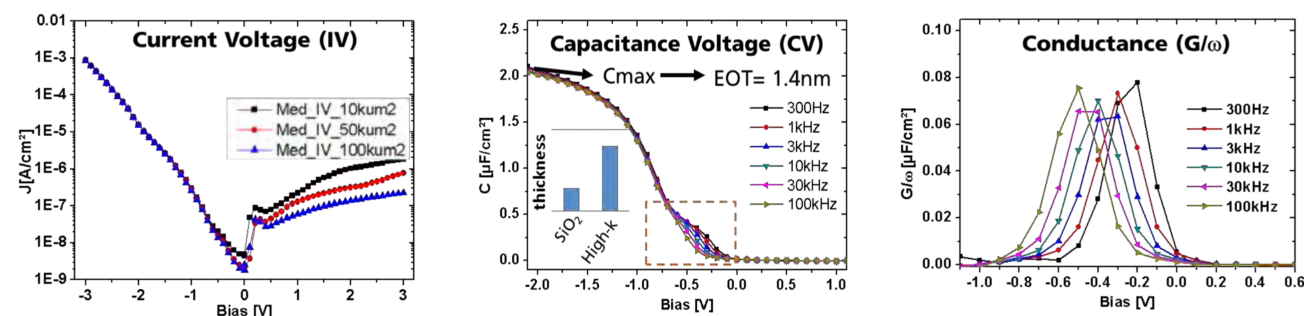
In early development phase or for very fast feedback loops the metal dot deposition on MIS/MIM stacks is the method of choice enabling fast electrical assessment of materials. Although a quite simple approach, it allows a large variety of different measurements including reliability testing with moderate statistics.

Being based only on small wafer pieces the drawback of this procedure is lacking information about wafer uniformity unless preparing multiple samples from different wafer spots. In an ion beam deposition tool a shadow mask on top of the sample projects defined metal electrodes (dots) of different size and shape onto the sample.
By means of specific preparation methods, the series resistance and contact to the chuck is reduced for optimum



2 Schematic cross section (left) and TEM cross-section (down) showing the integrated MIS material stack with magnification

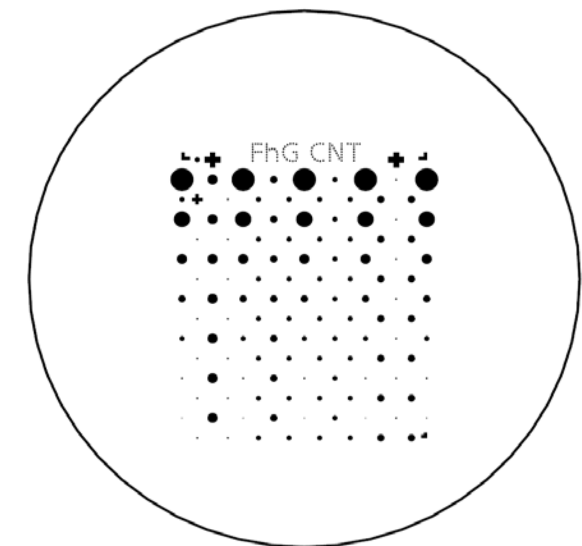
measurement results. When having an additional planar metal electrode on top of the dielectric further special treatments are required after dot deposition allowing also the characterization of complete MIM/MIS stacks with defined workfunction. The layout of the dot arrangement allows also automatic characterization of multiple dots with different size. Electrical results with error bars of current-voltage measurements in Figure 5 shows a good reproducibility of the measurements on different dots.

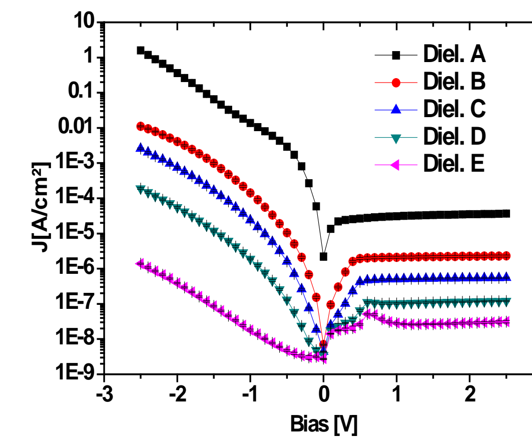


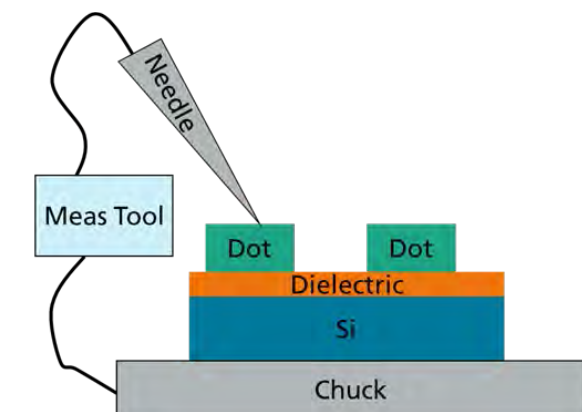
3 Electrical results of a high-k based MIS stack with (l) current voltage-, (m) capacitance-voltage- and (r) conductance characterisic

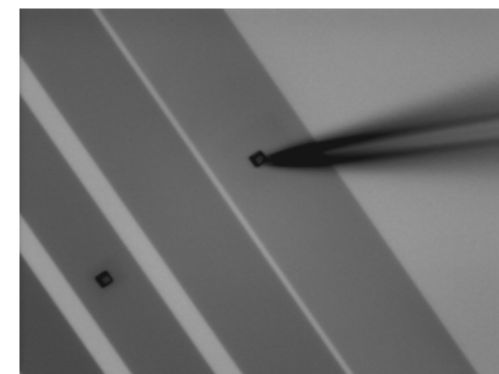
MIS/MIM trench capacitors short-loop

Researchers at Fraunhofer CNT developed a preparation and characterization method for MIS/MIM trench capacitors in order to understand the electrical performance of dielectrics and electrodes in 3D trenches in a very early technology development phase. This enables also evaluation of new materials and deposition processes at other research sites based on wafers or wafer pieces with trench arrays of different pitch and critical dimension. For electrical measurement, the trench arrays are equipped with small metal electrodes that are separated from other electrodes by an additional processing step (Figure 6). The characterization is carried out with tiny probe-needles. With this method, various electrical properties, like capacitance per trench or leakage characteristic can be investigated.









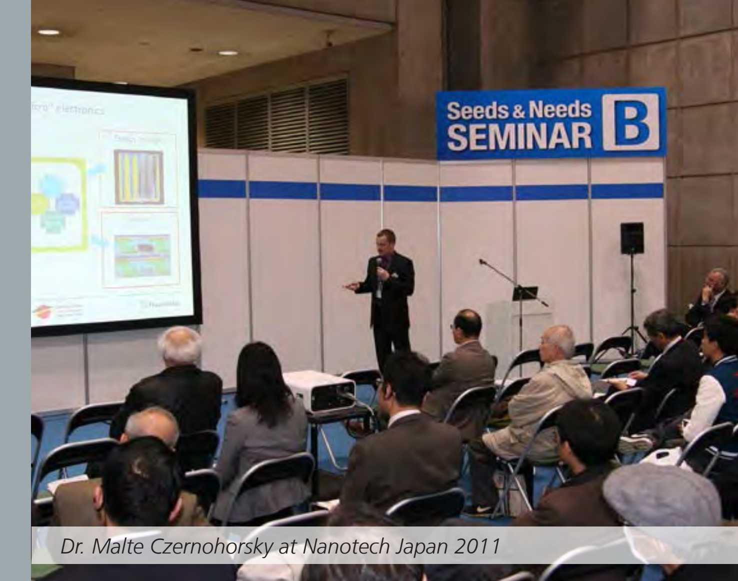
4 (top): Shadow mask layout (top) and schematic measurement setup (down) as example for dielectric characterization (MIS)

5 (top left): Current-voltage plots with error bars of different high-k dielectric material thicknesses

6 (left): Photograph of trench arrays having different pitch and dimension with metal electrodes (black) and probe-needle on contact

EVENTS

Torben Kelwing in the TechArena at the Semicon Europe 2011



Dr. Malte Czernohorsky at Nanotech Japan 2011

Fraunhofer CNT at Semicon Europe 2011

TRADE FAIR ACTIVITIES

Nano Tech	*February 16-18, 2011*	*Tokyo / Japan*
Silicon Saxony Day	*March 09, 2011*	*Dresden / Germany*
Semicon West	*July 12-14, 2011*	*San Francisco / USA*
Semicon Europa	*October, 11-13, 2011*	*Dresden / Germany*
Semicon Japan	*December, 07-09, 2011*	*Chiba / Japan*

Das Fraunhofer CNT präsentierte sich 2011 auf insgesamt fünf Messen und Ausstellungen mit den neuesten Entwicklungen.des Institutes.Besonders gefragt waren die Analytikleistungen des Fraunhofer CNT, vor allem die Atomsondentomographie sowie das energieautarke Sensorsystem. Erstmals in diesem Jahr war das CNT zweimal bei Messen in Japan vertreten, um Kontakte mit Industrievertreter zu intensivieren.

In 2011, Fraunhofer CNT presented its latest research results on five tradeshows and exhibitions.
The analytic services, like the atom probe tomography as well as the self-powered sensor system, were especially popular among the visitors.
For the first time, the CNT attended two trade fairs in Japan to intensify contacts with the local industry.

EVENTS

FRAUNHOFER CNT RESEARCH DAY 2011

Am 2. November 2011 fand der zweite Fraunhofer CNT Research Day statt. Spannende Vorträge von externen Experten und Wissenschaftlern des Fraunhofer CNT standen im Mittelpunkt dieses Tages. Es konnten wieder hochkarätige Referenten von Infineon, Air Liquide, ASM und weiteren bekannten Unternehmen der Mikroelektronik gewonnen werden. Neben den externen Vorträgen wurden Ergebnisse aktueller Forschungsarbeiten von Wissenschaftlern des Fraunhofer CNT vorgestellt.

Knapp 100 nationale und internationale Gäste aus Politik, Wirtschaft und Wissenschaft namen an der Veranstaltung teil..Aufgrund der wiederholt zahlreichen Teilnahme und dem positiven Feedback der Gäste hat sich der CNT Research Day fest in unserem Veranstaltungskalender etabliert.

The second CNT Research Day took place on 2nd November 2011. Recognized experts of leading companies in the microelectronics business, such as Infineon, Air Liquide and ASM, as well as scientific staff representatives of Fraunhofer CNT gave exciting talks on their latest research results and innovations.

About 100 national and international guests from politics, industry and science took part in the event. The large number of participants and the positive feedback show the success of the Research Day. Thus, it will become a regular event at the Fraunhofer CNT.

Lange Nacht der Wissenschaften

Am 1. Juli 2011 fand die 9. Dresdner Lange Nacht der Wissenschaften statt. Das Fraunhofer CNT präsentierte sich im Fraunhofer Institutszentrum auf der Winterbergstraße. Die Besucher des Standes konnten an einem Modell den Weg vom Sand zum Superchip verfolgen oder an einer Animation eine Reise in die Nanowelt antreten. Zusätzlich gab es die Möglichkeit, einen Chip unter einem Mikroskop unter die Lupe zu nehmen, sich in einem Reinraumanzug fotografieren zu lassen sowie sein Wissen in einem Quiz zu testen.

Night of sciences

The 9th Night of Sciences took place on 1st of July 2011. Fraunhofer CNT participated with a booth at the Fraunhofer institute center at Winterbergstraße. Visitors could follow the way „from sand to superchip“ on a model. They could experience a jouney into the world of nanoelectronics. They had the chance to examine microchips with a microscope or to slip in clean room clothes and to test their knowledge by participating in a quiz.

Friday@Fraunhofer

Am 24. Juni 2011 besuchten Schüler anlässlich des Friday@ Fraunhofer das Fraunhofer CNT, um an einem Vortrag sowie einer Window- und Labortour teilzunehmen. Bei einem Besuch des Reinraums konnten die Schüler eine Menge über die Forschung, z. B. im Bereich der Halbleiter, deren integrierte Schaltkreise mit Strukturbreiten unter 100 nm, die Charakterisierung von Materialien oder innovative Analyse- und Prozessmethoden lernen.

Friday@Fraunhofer

On June 24, 2011 pupils visited Fraunhofer CNT on the to listen to a lecture and to take part in a window and laboratory tour. During a visit in the clean room, students learned a lot about research, they got information about semiconductors, integrated circuits with dimensions below 100 nm, material characterization or innovative analytical and process methods.

Promotionen am CNT

Im Jahr 2011 konnten wir zwei unserer Mitarbeiter zu ihrer Promotion beglückwünschen.
Frau Dr. Romy Liske verteidigte ihre Dissertation mit dem Thema: "***Die Kinetik der elektrochemischen Kupferabscheidung in Sub-100 nm-Strukturen***". Romy Liske ist seit 2011 Gruppenleiter des Bereiches Functional Electronic Materials: Back-End of Line am Fraunhofer CNT.
Herr Dr. Sergej Mutas verteidigte seine Dissertation mit dem Titie ***„Analysis of high-k materials with Local Electrode Atom Probe“.*** Dr. Segej Mutas ist nach seiner erfolgreichen Verteidigung zu Globalfoundries gewechselt.

Doctorates at CNT

In 2011, two of the Fraunhofer CNT scientists were able to complete their dissertations.
Mrs. Romy Liske defended her thesis with the topic: "***The kinetics of electrochemical deposition of copper in sub-100 nm structures***". She is now working as group manager of the competence area Functional Electronic Materials: Back-End of Line at CNT.
Mr. Sergej Mutas completed his thesis on "***Analysis of high-k materials with Local Electrode Atom Probe“*** and is now working for Globalfoundries.

EVENTS

COLLOQUIA

17.01.2011
48th Fraunhofer CNT Kolloquium
Prof. Joo-Hyung Kim
"New electronic material: Cellulose for electronics"

08.02.2011
51st Fraunhofer CNT Kolloquium
Prof. Horst Hahn, KIT
"Nano-Forschung am KIT – Kooperationskonzept"

20.01.2011
49th Fraunhofer CNT Kolloquium
Dr. Frank Schwierz, TU Ilmenau
"Graphen - das Material für die Elektronik von morgen?"

31.03.2011
52nd Fraunhofer CNT Kolloquium
Jan Sickmann, TU Dresden
"Mapping nanofields in semiconductors by off-axis electron holography"

25.01.2011
50th Fraunhofer CNT Kolloquium
Mayrita Arrandale, Atotech USA Inc.
"Microbial Bioremediation of Heavy Metal Containing CMP Wastewater"

13.09.2011
53rd Fraunhofer CNT Kolloquium
Dr. Torsten Feigl, Fraunhofer Institut für Angewandte Optik und Feinmechanik, Jena
"EUV multilayer optics"

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Comparative study of far-field and near-field Raman spectra from silicon-based samples and biological nanostructures
In: Journal of physical chemistry. C, Nanomaterials and interfaces 115 (2011), Nr.50, S.24512-24520

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Analyse und Vergleich professioneller Software zur Festplattenverschlüsselung anhand von Verschlüsselungsmethoden und Handhabbarkeit zur Absicherung tragbarer Computer
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Take the bus line 77 from Dresden-Airport and leave at the stop "Infineon". Change to the tram line 7 towards "Pennrich". Get off at the stop "Infineon Süd". From here it is only a 3-minute-walk to building 48.

By car:
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EDITORIAL NOTES

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