Fraunhofer

IPMS

FRAUNHOFER INSTITUTE FOR PHOTONIC MICROSYSTEMS IPMS
CENTER NANOELECTRONIC TECHNOLOGIES (CNT)

| CUSTOMER APPLICATION & DESIGN |
| LAYOUT & DATA PREPARATION | LITHOGRAPHY | PATTERNING | CUSTOMIZED DEVICE |

Process chain at Fraunhofer IPMS-CNT

| MATERIAL SUPPLIERS | IC MANUFACTURERS |
| EQUIPMENT MANUFACTURERS | BASIC RESEARCH INSTITUTIONS |

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E-BEAM LITHOGRAPHY & ETCH

DEVICES & VALUE ADDED SOLUTIONS | ANALYTICAL SERVICES | SCREENING FAB SERVICES

NANOPATTERNING

Creating nano-scale structures is necessary for a wide range of applications in the semiconductor business. Key challenges are creating precisely controlled patterns with small dimensions, flexible and adaptable layout generation and processes as well as uniform and reproducible wafer-scale integration.

Fraunhofer IPMS business unit CNT offers state-of-the-art nanopatterning capabilities using electron beam direct write lithography and reactive ion etching. Thus, customized structures with sizes below 40 nm can be created on a variety of wafer sizes and substrate types.

Starting from the customer's design the whole package involving layout generation and modification, data preparation, e-beam lithography, pattern transfer using etch processes together with the needed in-line metrology and analytics up to separation into single chips is offered.

APPLICATION EXAMPLES

- Fabrication of test structures for technology development
- Structuring of Application Specific Integrated Circuits (ASICS)
- Design tests of innovative devices and cell concepts and their variation on a wafer (Chip Shuttle)
- Calibration pattern for metrology development
- MEMS and NEMS patterning with productive quality
- »Mix & Match« with optical exposure techniques
- Optical gratings and light modulation devices
- Correction of design or process errors in finalized CMOS structures (Metal Fix)
- High aspect ratio patterning (TSV, 3D capacitors)
- Nanoimprint masters

Vistec SB3050DW variable shaped E-beam for direct maskless patterning

TEL ACT 12 Clean Track for fully automated 12" coating and development

Tokyo Electron Mainframe with VIGUS chamber (specifications see below)

ADVANTAGES AT CNT

- *Realization of customer specific patterning from sketch to etch*

- *Direct maskless patterning*

- *Structuring without optical diffraction limit below 40 nm (half pitch)*

- *Exposure of various designs or layout variations on single wafer, mix&match*

- *Different etch capabilities (e.g. ICP, CCP, high-T, MW)*

- *Wide range of inline-metrology and analytics available (patterned defect inspection, TEM, AFM and many more)*

- *ISO 9001 certification for high quality industrial services*

- *Professional contamination management and fast wafer exchange*

- *Close industry connection and vast collaboration network (foundries, supplier and universities) with over 10 years of experience*

EQUIPMENT - LITHOGRAPHY

- **E-beam - Vistec SB3050DW**

  Wafer sizes: 4", 6", 8" & 12"

- **Clean Track - TEL ACT 12**

  - Fully automated 12" coating and development
  - Processing of chemically amplified resists (CAR) and non-chemically amplified resists
  - Resist evaluation

- **CD-SEM - AMAT Verity 4i**
- **Optical inspection - Leica INS3300**
- **BF/DF Patterned Wafer Inspection System - NextIn AEGIS**
- **Unpatterned Wafer Defect Inspection**
- **Systems - KLA Surfscan SP2 & SP3**

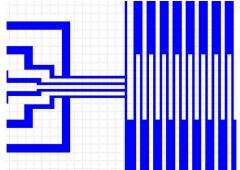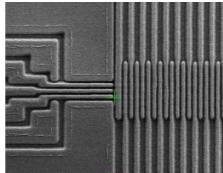 Wafer sizes for metrology tools: 8" & 12"

EQUIPMENT - ETCH

Tokyo Electron and Applied Materials Mainframes for 12" Wafer (BEOL and FEOL):

- ICP and CCP reactors with RF pulsing options
- Gas pulsing and ALE processing
- High temperature etching (up to 250 °C)
- Highly flexible process gas selection
- Optional 8" wafer processing
- In-situ plasma analytics (QMS, SEERS, HROES)

Applications:

- Nanopatterning with critical dimension (CD) below 20 nm
- High aspect ratio etching at CDs <1 μm
- Dual damascene lowK patterning
- Etching of various materials
  - Standard materials:
    Substrate Si, poly-Si, amorphous Si
  - Hard mask materials: SiN, SiO_2
  - Metal gate materials: TiN, TaN, W, WSi
  - High-k Materials (at 250 °C):
    Al_2O_3, HfO_2, SiHfOx, ZrO_2
  - Metal: Al, AlSi, AlCu, AlSiCu

▲ *Nanostructure as designed (left) and after e-beam nanopatterning and etching (right). Smallest pitch 80 nm, trench width 28 nm. In cooperation with Infineon Dresden, RWTH Aachen, and FZ Jülich.*