

TSN-EP | ETHERNET TSN ENDPOINT CORE

Time-Sensitive Networking (TSN) enhances the Ethernet specification towards time synchronization and deterministic communication (specifically IEEE 802.1 and 802.3). The goal is it to make Ethernet more suitable for the advancing needs of industrial and automotive applications. The TSN Ethernet IP core TSN-EP eases the integration of devices into networks complying with the TSN standards. It provides time-sensitive networking for full duplex point-to-point Ethernet communication. The IP core consists of three sub-modules for time synchronization, traffic shaping and low latency Ethernet MAC communication.

More than 150 customers worldwide have relied on the quality of Fraunhofer IPMS IP-Core solutions for FPGA and ASIC designs and the comprehensive technical support for over 10 years.

Applications

The TSN-EP IP Core is suitable for the implementation of talkers and listeners within TSN Ethernet networks requiring time synchronization as well as robust, low-latency, and deterministic communication.

It is targeting for applications in industrial automation, robotics, automotive, aerospace and more.

Verification

Interoperability of sub-modules is constantly tested within TSN plug-fests by LNI 4.0 and Industrial Internet Consortium (IIC).



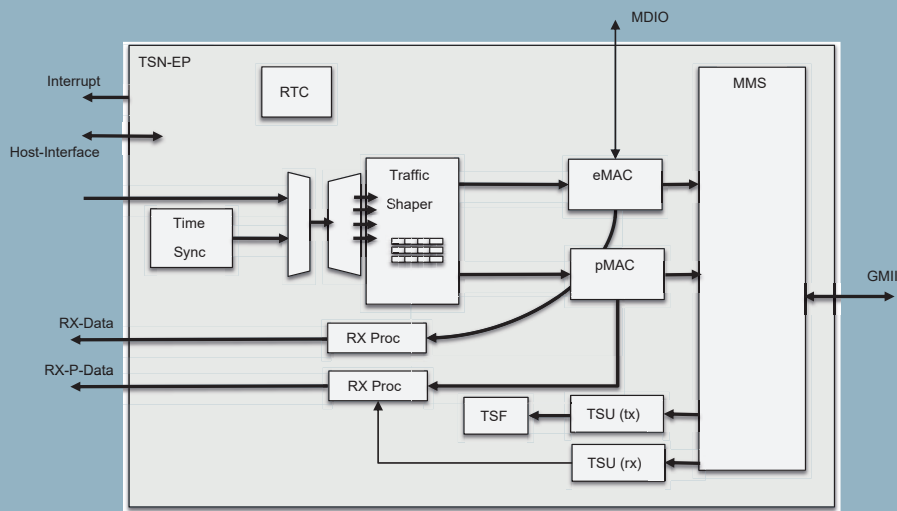
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Schematic diagram of the TSN-EP.

TSN Features

- Time synchronisation (IEEE 802.1 AS-2020)
- Traffic-Shaping (IEEE 802.1 Qav and Qbv)
- Frame Preemption (IEEE 802.3br and IEEE 802.1Qbu)
- Frame Replication and Elimination (IEEE 802.1CB)
- SRP Enhancements (IEEE 802.1Qcc)
- Stream Filtering and Policing (IEEE 802.1Qci)
- Cyclic Queuing and Forwarding (IEEE 802.1Qch)
- Ethernet MAC communication (IEEE 802.3)
- Specialized DMA-core on request

Easy Integration

- Platform independent implementation Xilinx, Intel, Microsemi, Lattice, Gowin FPGAs and any foundry technology
- Intel Altera based evaluation platform
- Xilinx based evaluation platform
- Set of demo projects for Xilinx
- Altera configurable featureset
- Optimized for multiport bridging operation
- ASIC & FPGA design support
- TSN Evaluation Kit available

Interfaces

- Advanced Peripheral Bus (APB) for memory mapped register access
- 2 – 8 AXI-Streams for TX data (configurable byte width)
- 1 AXI-Stream for RX data (configurable byte width)
- Avalon interfaces available
- PHY: MII, GMII, RGMII

Deliverables

- Verilog RTL source code or targeted FPGA netlist
- Testbenches
- Sample simulation and synthesis scripts
- Comprehensive documentation
- PTP software stack in plain C as source code or precompiled library
- FreeRTOS example projects
- Linux driver and example
- TSN network configuration examples

Designed for Usage with Ethernet MACs

- ALTERA/Intel Triple Speed Ethernet MAC
- XILINX Tri-Mode Ethernet MAC
- IPMS Triple Speed Low-Latency Ethernet MAC
- Triple speed: 10 / 100 / 1000 Mbit/s Ethernet
- 2.5/5/10+ Gbps on request



TSN Evaluation Kit: Netleap board (Intel / Altera); implemented IPMS TSN-IP core for endpoint applications (TSN-EP).