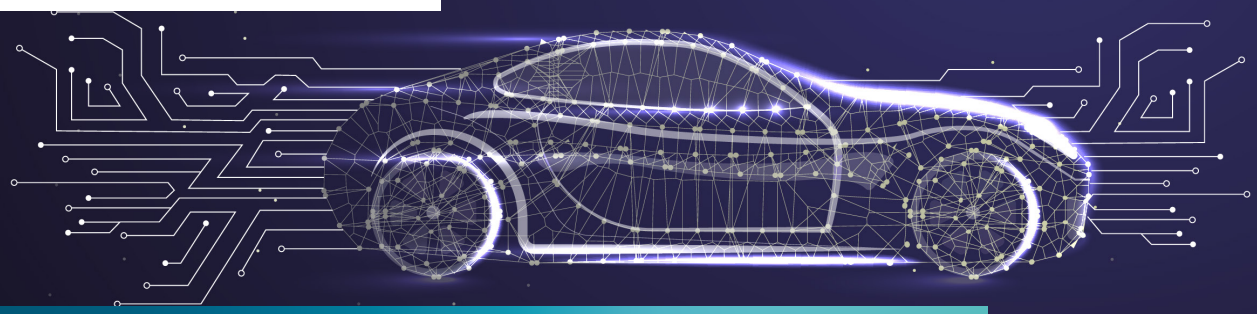
Fraunhofer IPMS



EMSA5-FS – RISC-V Functional Safety Processor IP Core

EMSA5-FS is ASIL-D ready for functional safe system development according to ISO 26262 "Road vehicles – Functional safety". It is a 32-bit, in-order, single-issue, five-stage pipeline processor supporting the open standard RISC-V instruction set architecture (ISA). Its fail-safe features include built-in triple or double modular redundancy (with lockstep), error correction code (ECC) protection of buses, a configurable memory protection unit, privileged operation modes, and Reset and Safety Manager Modules. It can be used for ASICs or FPGAs, and as either a stand-alone processor or pre-integrated in optional subsystems combining a bus fabric with typical peripherals.

Benefits

- ASIL-D ready certified according to ISO 26262
- Supported by ISO 26262 and IEC 61508 certified toolchain (IAR Systems Workbench) enables simplified development and certification of safety-critical systems
- Triple Mode Redundancy for airborne operation
- IP Core available for any FPGA type and ASIC design

Applications

The EMSA5-FS core is suitable for implementing microcontrollers for devices and systems in automotive, airborne, space, medical and other safety critical applications.

Key Features

- 32-bit, 5-stage pipeline architecture
- Low footprint and high frequency
- RV32I and and RV32E RISC-V standard compliant
- Privileged Instructions: Machine (M) and User/Application (U)
- Physical memory protection (PMP)
- Hardware trigger module and performance counter
- RISC-V complient debug interface
- PLIC - Platform Level Interrupt Controller
- AHB-lite Interface

Easy System Integration

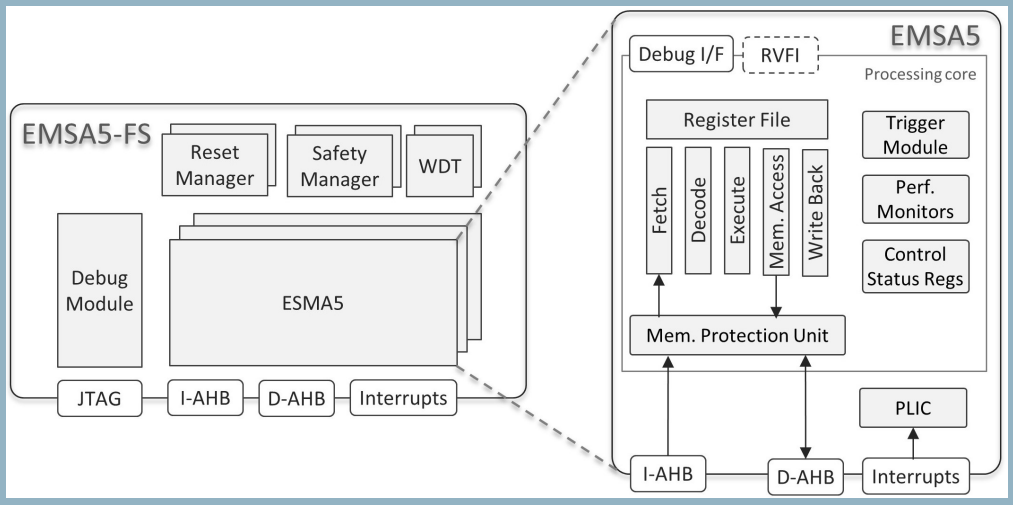
- Platform independent implementation Xilinx, Intel, Microsemi, Lattice, Gowin FPGAs and any foundry technologies
- Responsive implementation support

Contact

Monika Beck
+49 351 88 23 - 274
monika.beck@ipms.fraunhofer.de

Fraunhofer Institute for
Photonic Microsystems IPMS
Maria-Reiche-Str. 2
01109 Dresden
Germany

www.ipms.fraunhofer.de



Peripheral Package

- I2C
- SPI
- QSPI
- Timer
- UART
- Watchdog
- GPIO
- AHB/APB SRAM/SDRAM controller-PWM

Compliance to RISC V Specification

- Instruction Set Manual
  - Volume 1, latest Unprivileged Spec
  - Volume 2, latest Privileged Spec
- External Debug Support

Interfaces

- AHB-Interconnect
- AHB-to-APB4 bridge
- APB-Interconnect
- AHB-to-AXI4-Lite
- AHB Multi Master/Layer Interconnect (MLIC)

Toolchain

- IAR Embedded Workbench
- Lauterbach TRACE32® trace and debug toolset
- GNU Compiler Collection (GCC) + Open OCD + Eclipse
- Trigger-Module (HW-Breakpoints) Command line
- JTAG Debug Support

RISC-V Development Boards

- Arty A7 (Xilinx)
- DE10-Standard (Intel)

Functional Safety

- ISO 26262 ASIL-D ready certified
- Redundancy and Safety:
  - Dual-mode and triple-mode redundancy
  - Dual-mode redundancy with optional Lockstep
  - Safety manager
  - Safety watchdog
- Functional safety based software development compliant to IEC 61508 and ISO 26262 using IAR Workbench
- Complete certification package including FMEDA and SAM documents
- Memory protection unit with up to 16 regions of configurable size

Debug Features

- Configurable Hardware Performance Monitor
- Supports for RISC-V External Debug Interface
- Configurable Trigger Module
- Optionally delivered with an Advanced Integrated JTAG Debug Controller

Deliverables

- System Verilog RTL source code or targeted FPGA netlist
- Sample simulation and synthesis scripts
- Software example projects
- Comprehensive documentation
  - Design Specification
  - Integration Manual
  - Safety Manual
  - FMEDA
  - Release Notes
  - Test Verfication Document
  - Software User Guide
  - Peripheral User Guide
  - Processor User Guide

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