Fraunhofer
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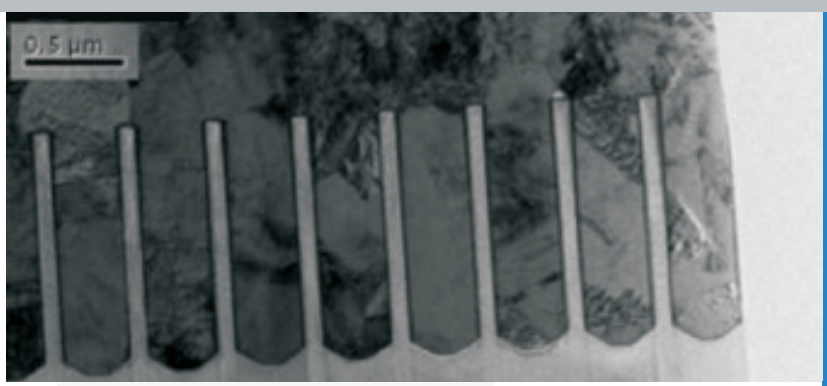
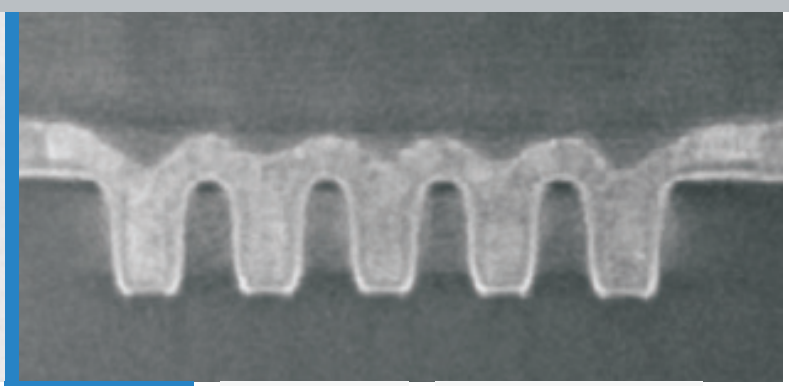
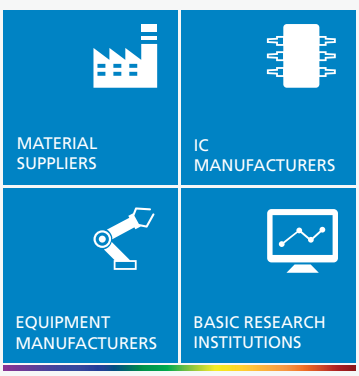
FRAUNHOFER INSTITUTE FOR PHOTONIC MICROSYSTEMS IPMS





INTERCONNECTS | HIGH-K DEVICES | NON-VOLATILE MEMORIES



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IN COOPERATION WITH
GLOBALFOUNDRIES | IHM Dresden

ULTRA-LOW-K / COPPER INTERCONNECTS

TASK DEFINITION

The use of copper as wiring material in the semiconductor industry revolutionized the metallization process and contributed substantially to launch faster, smaller and less energy consuming processors and integrated circuits.
On the one hand, this progress can be attributed to changed process technologies, allowing more complex multi-layered interconnects. On the other hand, it is the electrical property of copper itself which leads to processor performance improvement.

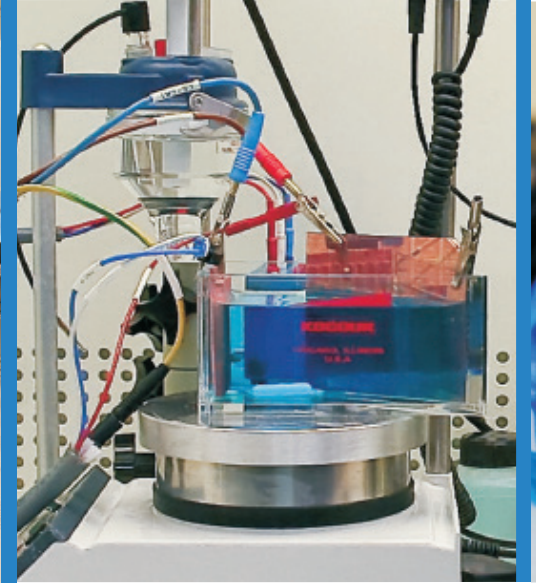
METHODOLOGY

At the Fraunhofer IPMS a fully equipped 300 mm BEoL process line was launched, which comprises ultra-low-k (ULK) dielectric etch and repair processes, various barrier/seed deposition techniques, copper plating and chemical-mechanical planarization (CMP) processes.
Process development is focused on sub-45-nm technology nodes on 300 mm wafers. Research work is carried out within the scope of governmental funded projects and in close cooperation with the Semiconductor and Microsystems Laboratory at Dresden University of Technology and GLOBALFOUNDRIES.

TECHNICAL DATA

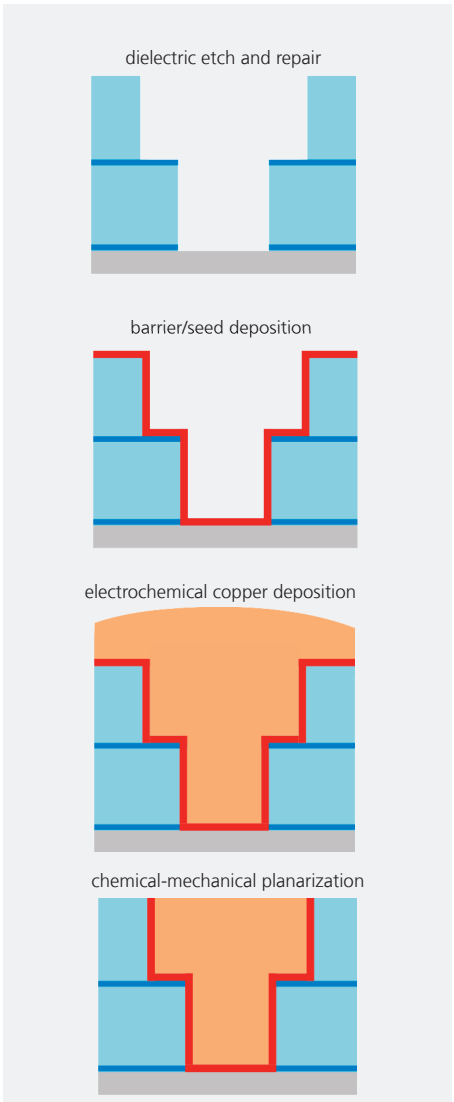
- ULK etch: Advanced etch Applied Materials Centura
- ULK repair: Advanced Wet Clean Semitool Raider
- Barrier/seed deposition: Applied Materials Endura2
- Copper plating: Semitool Raider
- Copper anneal: TEL Formula
- CMP: Applied Materials Reflexion LK

CNT cleanroom with ULK, copper plating CMP tools.



Temperature controlled copper plating experiments on wafer coupons in a Hull cell

Chemical screening for copper plating electrolytes



300-mm-BEoL-integration line at Fraunhofer IPMS

ADVANTAGES

- Production-like research facility
- Fast process optimization and integration
- Implementation of feasibility studies on 300 mm wafers, partly on 200 mm wafers and coupons
- Maskless preparation of test-layouts via e-beam direct write technology
- Possibility of pre- and post-processing at established Silicon Saxony companies
- Intense research and industrial cooperation with the Dresden University of Technology and GLOBALFOUNDRIES

APPLICATIONS

- Etch damage repair in ultra-low-k structures
- Development of barrier/seed films (TaN/Ta, Co, Ta(N) Ru and other materials)
- Process development (PVD, CVD, ALD, ECD; Anneal)
- Seed layer enhancement, direct on barrier plating (Cu)
- Electrochemical investigations (cyclic voltammetric stripping, electrochemical impedance spectroscopy)
- Chemical screening for repair, CVD, ALD, plating and CMP

ANALYTICS

- **Ellipsometric porosimetry:** Measuring of porosity, pore size and distribution of open pore systems, pore diameter > 0.5 nm; determination of lateral diffusion coefficients
- **Ellipsometry:** Measuring of optical parameters of thin films with optional mapping; enhanced spectral range up to 1700 nm
- **XPS:** In situ analysis of barrier/seed composition; ex situ film analysis
- **AFM:** Surface topography measurement, critical dimension (CD) analysis, side wall roughness, 300 mm and 200 mm capable
- **FIB-SEM, TEM:** Defect and CD analysis, line edge roughness, surface imaging
- **High resolution profilometry:** Investigation of surface profiles and roughness
- **4-point resistivity measurement:** Resistivity mapping of metallic films on 300 mm wafers
- **XRD/XRR:** Texture analysis, evaluation of stress, density, grain size, grain orientation and roughness, temperature-controlled stage up to 950 °C for crystallization temperatures determination
- **SIMS:** Quantitative elemental analysis and depth profiling, dynamic or static mode
- **Atom probe:** Three-dimensional quantitative elemental analysis with atomic resolution

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