An underestimated design related product reliability risk from plasma processing induced charging damage - PID

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Abstract: Plasma processing induced charging damage (PID) is a serious reliability risk for designs of integrated circuits of various processing nodes and several device types. Dependent on the type/style of design the sensitivity to PID can vary significantly. The most prominent degradation is reported for MOS transistors, but also integrated capacitors can suffer degradation or even dielectrics between metal lines in the metal stack. Any type of technology can be affected implemented on bulk-silicon or on SOI with dielectrics such as SiO_2 as well as high-K materials. The reliability risk for a productive circuit is supposedly eliminated by so-called antenna design rules. The maximum metal area causing the charging event is limited in the design manual. However the antenna design rules are only sufficient when the PID reliability stress characterization throughout the process qualification has a high grade and is complete. The incorporation of all possible degradation modes for the PID failure mechanism is essential but not necessarily accomplished. The open question is: “Are all PID risks covered by the rules in the design manual?”

In this tutorial the PID-basics such as antenna ratio, electron shading effect etc. are described briefly and furthermore pitfalls and new findings are highlighted, which could cause significant product risks depending on the layout style. An important topic are the protective devices against PID, their effectiveness is discussed. Aspects associated with 3D-systems are illustrated with respect to PID. Also the limitations of design rule checkers and circuit routing tools are described. The tutorial will give the “beginner” an introduction to the PID-topic while the advanced scientists gets a further perspective into the more or less hidden problem areas.

Andreas Martin received his M.Eng.Sc. in Electrical and Electronic Engineering from the Technical University of Darmstadt, Germany, in 1992. After six years in the silicon technology characterization group of the research center “Tyndall Institute” (former NMRC), Cork, Ireland he started working for the corporate reliability department of Infineon Technologies AG in Munich, Germany in the field of fWLR Monitoring (reliability monitoring on product wafers). He is involved in advanced and novel test structure design, development of new stress methods and data analysis techniques on the topics: dielectrics, plasma induced damage (PID), metallization and MOS device degradation for a wide range of processing nodes. He is responsible for the PID process qualification and plasma charging design manual rules at Infineon worldwide. He has published and co-authored numerous papers/presentations, some patents, given tutorials and invited talks at various conferences and served in committees of the IEEE IRW, IEEE IRPS, ESREF and of the “Workshop on Dielectrics in Microelectronics” (WoDiM) for many years. He is involved in paper reviews for several journals. He is a senior member of the IEEE, Infineon´s alternate of the JEDEC-subcommittee 14.2, member of the IEC WLR-workgroup TC 47 and co-chair of the German ITG-group 8.5.6 on “WLR and reliability simulations”. Currently, he is moderating two JEDEC working groups on: 1) Definition of a standard on PID stress measurements and PID reliability analysis; 2) Guideline on fast Wafer Level Reliability (fWLR) Monitoring on product wafers.