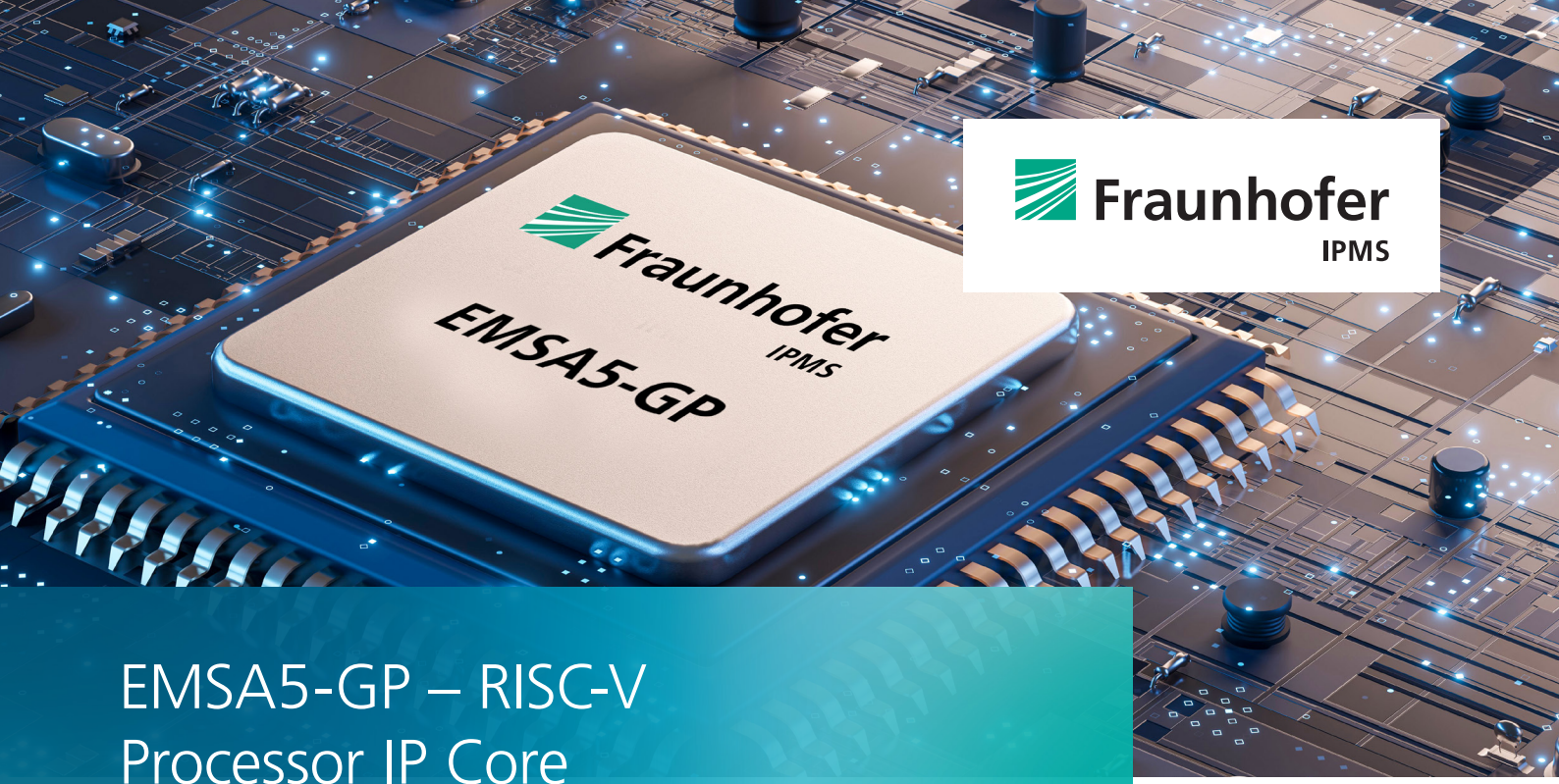


Fraunhofer IPMS

EMSA5-GP – RISC-V Processor IP Core

The EMSA5-GP RISC-V Processing Core is a RISC-V-compatible processing unit which supports the RISC-V 32-Bit ISA and the privileged instruction set. The design guiding principles are small footprint and high frequency making the core suitable for embedded systems as well as data communication SoCs. EMSA5-GP is available for ASICs or FPGAs, and as either a stand-alone processor or pre-integrated in optional subsystems combining a bus fabric with typical peripherals.

Key Features

- 32-bit, 5-stage pipeline architecture
- Low footprint and high frequency
- RV32I and RV32E RISC-V standard compliant
- Privileged Instructions: Machine (M) and User/Application (U) Mode
- Physical memory protection (PMP)
- Hardware trigger module and performance counter
- RISC-V compliant debug interface
- PLIC - Platform Level Interrupt Controller
- AHB-lite Interface

Applications

The EMSA5-GP core is suitable for deeply embedded applications, Edge Computing, Embedded IoT, Edge AI, networking and data communications.

Contact

Monika Beck
+49 351 88 23 - 274
monika.beck@ipms.fraunhofer.de

Fraunhofer Institute for
Photonic Microsystems IPMS
Maria-Reiche-Str. 2
01109 Dresden
Germany

www.ipms.fraunhofer.de

Peripheral Package

- MSSP (SPI, I²C)
- QSPI
- Timer
- UART
- Watchdog
- GPIO
- AHB/APB SRAM/SDRAM controller-PWM

Compliance to RISC V Specification

- Instruction Set Manual
  - o Volume 1, latest Unprivileged Spec
  - o Volume 2, latest Privileged Spec
- External Debug Support

Interfaces

- AHB-lite single layer interconnect
- AHB-lite multilayer interconnect
- AHB-lite to AXI4-lite bridge
- AHB-lite to AXI4-lite to APB CDC bridge

Toolchain

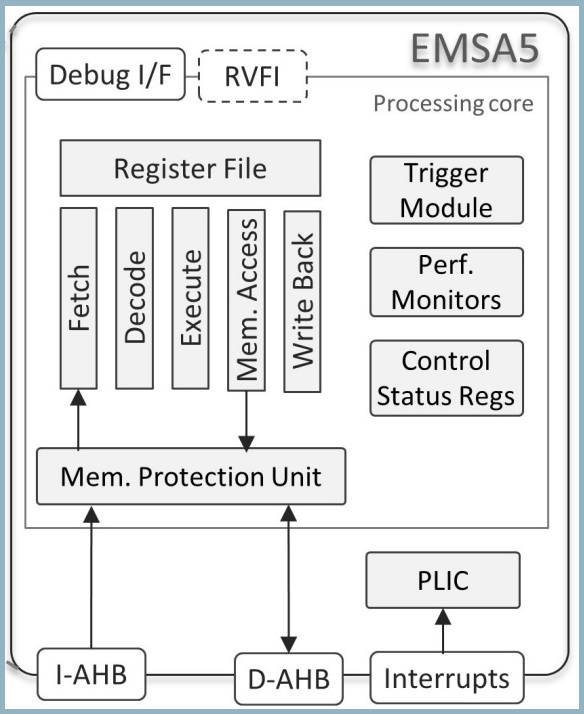
- IAR Embedded Workbench
- Lauterbach TRACE32® trace and debug toolset
- GNU Compiler Collection (GCC) + Open OCD + Eclipse
- JTAG Debug Support
- LLVM/Clang on request

RISC-V Development Boards

- Arty A7 (Xilinx)
- DE10-Standard (Intel)

Easy System Integration

- Platform independent implementation into any FPGA or foundry technologies
- Responsive implementation support



Debug Features

- Configurable Hardware Performance Monitor
- Supports for RISC-V External Debug Interface
- Configurable Trigger Module
- Optionally delivered with an Advanced Integrated JTAG Debug Controller

Deliverables

- System Verilog RTL source code or targeted FPGA netlist
- Sample simulation and synthesis scripts
- Software example projects
- Comprehensive documentation
  - o Design Specification
  - o Integration Manual
  - o Release Notes
  - o Test Verfication Document
  - o Software User Guide
  - o Peripheral User Guide
  - o Processor User Guide